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CONCEPT STUDY FOR UHF T/R MODULES

Georgia Institute of Technology

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This report discusses issues related to the performance and producibility of ultrahigh frequency (UHF) transmit/receive modules for phased array radar. The main issues are improved power devices, combining methods, balanced circuitry, optimization of integration, and post-assembly adjustment. These issues are summarized in an investment strategy for UHF.

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SUMMARY

This report discusses some important issues related to the performance and producibility of ultrahigh frequency (UHF) transmit/receive modules. Unfortunately, there are a number of factors which currently limit precision phase and gain tracking between such modules. Some of this variability results from imperfections in the modules themselves while other contributors are a consequence of the very nature of the array environment. An analysis of these issues, with a concomitant identification of the major gaps in the knowledge base of the underlying technologies, permits the development of an "investment strategy" for UHF. Some pillars of this strategy involve the use of transistors at lower frequencies, a re-visiting of balanced circuitry, the development of both improved power devices and methods to power combine such devices, an optimization in the level of integration and the incorporation of post-assembly tweaking techniques for module manufacturing. Augmenting these activities with enhancements in both open-loop and closed-loop module control should help permit the deployment of phased array radars with performance envelopes well beyond the current state-of-the-art.

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1.0 INTRODUCTION

This report discusses some important issues related to the performance and producibility of ultrahigh frequency (UHF) transmit/receive modules. An analysis of these issues and an identification of the major gaps in the knowledge base of the underlying technologies permits the develoment of an "investment strategy" for UHF.

The transmit/receive (T/R) module is an important component of a phased array radar system. Phased array radars scan a surveillance region by electronically steering the beam, rather than by physically rotating the antenna. The requisite electronic steering is a consequence of adjusting the phase of each of the waveforms transmitted by the constituent radiating elements in the phased array.[1,2] In regions where the respective maxima of the waves coincide, constructive interference occurs and a strong signal results. At selected other locations, however, the waveforms are exactly out of phase. In these regions, destructive interference occurs and this causes a cancellation of the aggregate signal. For example, if all of the individual wavefronts leaving the antenna platform are exactly in phase, the resulting signal will be strongest in a direction perpendicular to the plane of the antenna face. Consequently, in this configuration, the radar is aimed to detect echoes from targets straight in front of the antenna as illustrated in Figure 1. However, if a phase delay is introduced across the face of the radiating elements, then the radar is best suited to detect objects off to one side of the perpendicular axis. In practical radars, this phase-lag steering enables a fixed-position, phased array radar to deflect its beam up to about 60 degrees from its perpendicular axis.[1] Furthermore, the steering can be performed in a tiny fraction of a second and, thus, the same antenna can be used to track many objects simultaneously.

The electronics which help to produce this phase-lag steering and which, in addition, rapidly switch the system from a radiating to a transmitting mode are generally contained in a T/R module.[3]

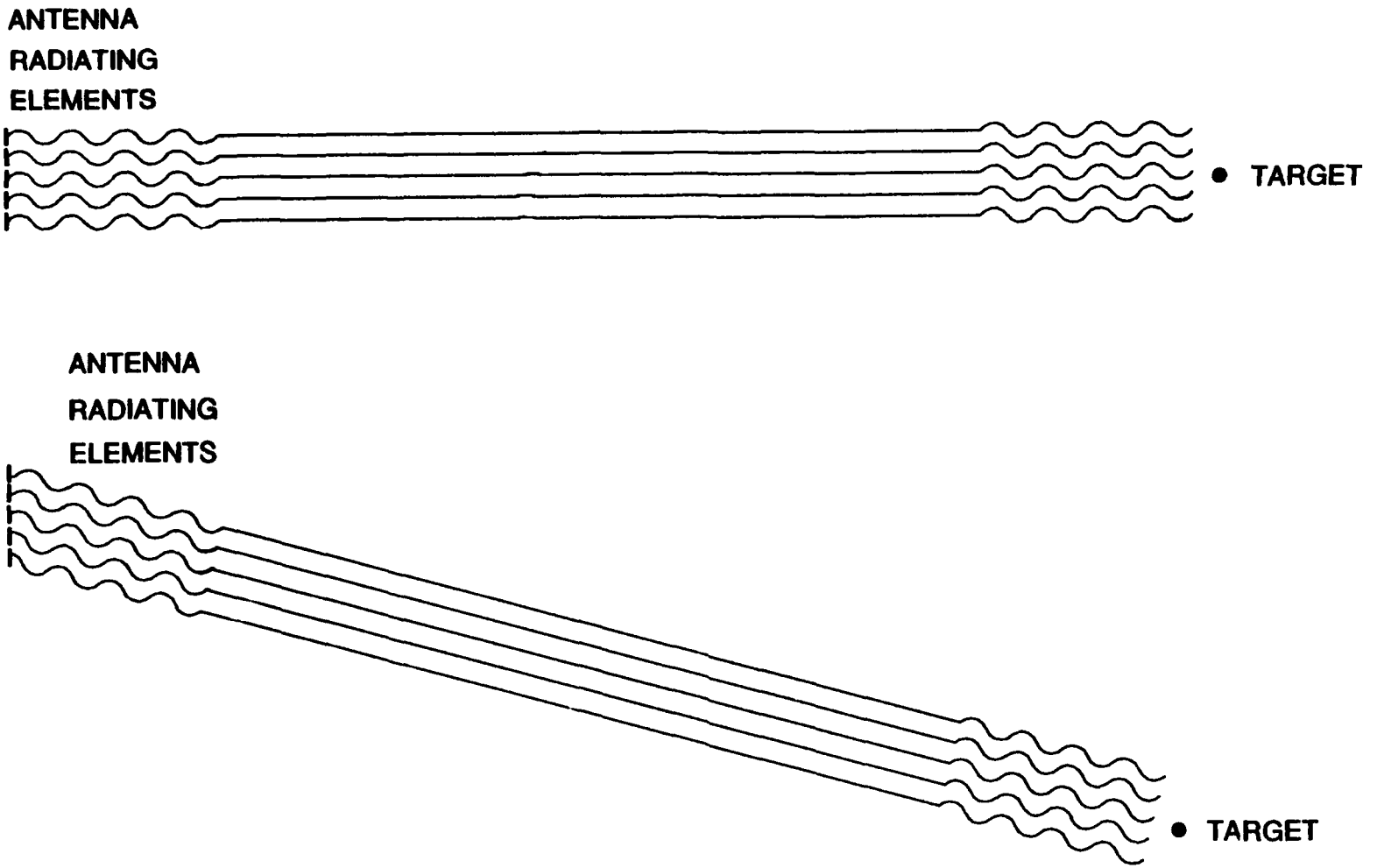

Figure 1. An Illustration Of How An Array Of Radiating Elements Operating With Respective, Systematic Phase Delays Can Steer The Corresponding Radar Beam. (After Brookner, Ref. 1).

A block diagram for a typical module is shown in Figure 2 and a summary of the constituent components is presented in Table 1. A number of technologies are available for constructing such modules and five approaches germane to UHF radars are enumerated in Table 2. A manufacturer makes a selection from this menu based upon the transmit power requirements, the frequency of operation, the environment in which the radar will be deployed, his previous investment in similar production tooling and, perhaps, the demeanor of his technical and management personnel. It is generally conceded that the technology selection "rules of thumb" described in Table 3 are implicitly applied by the majority of module manufacturers.

Regardless of the selected technology, the evaluation criteria for the modules themselves seem to involve some, or all, of the items elucidated in Table 4. The necessity of good amplitude and phase tracking between modules is particularly important for the present contract and considerable attention has been devoted to the factors which are currently limiting their achievement.

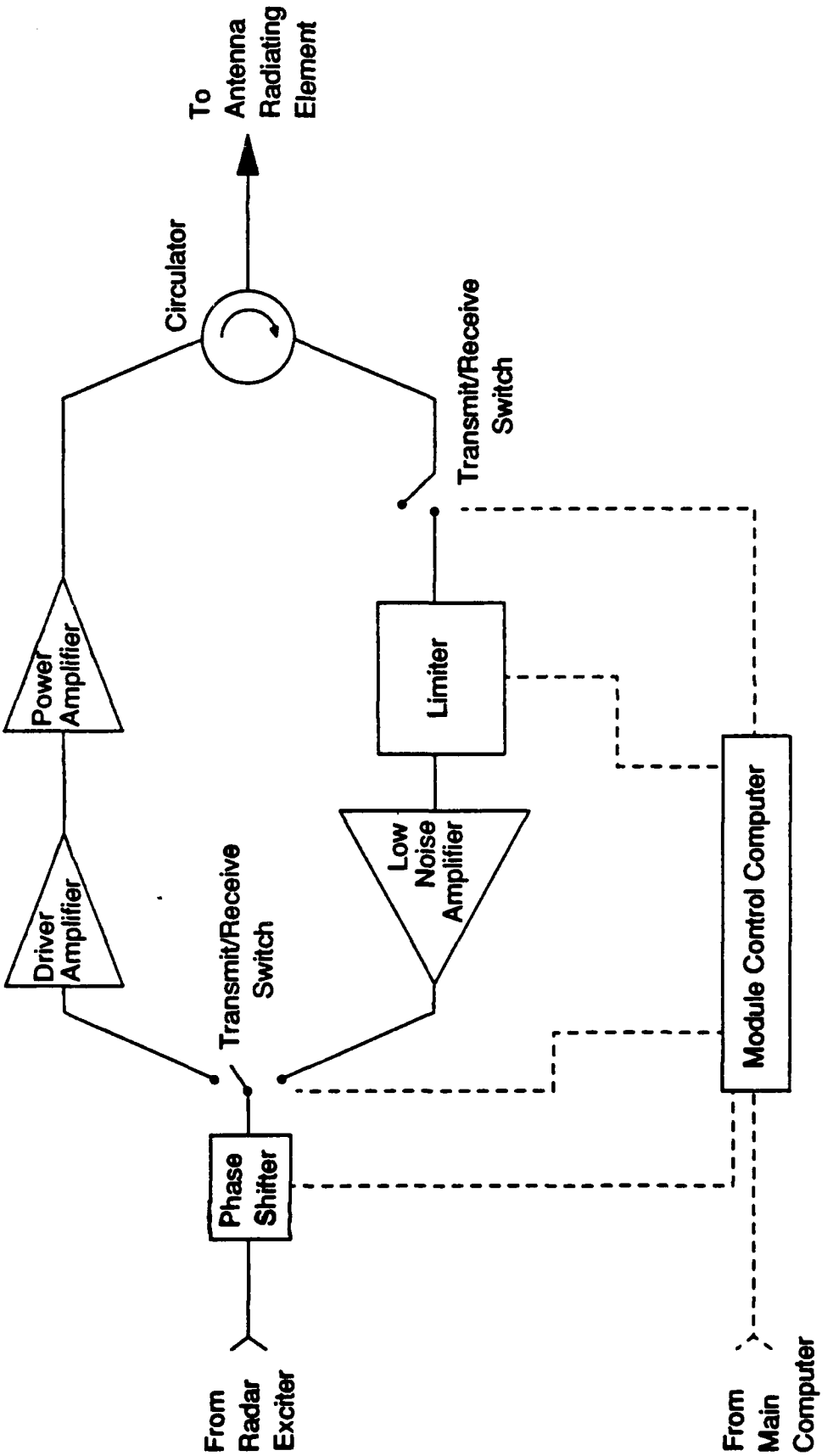

Figure 2. Schematic Representation Of A Typical Transmit/Receive Module.

Phase Shifter

Transmit/Receive Switches

Driver Amplifier

Power Amplifier

Circulator

Limiter

Low Noise Amplifier

Module Control Computer

Table 1. Basic Components Of A Typical Transmit/Receive Module.

Tubes And Conventional Microwave-Type Plumbing

Hybrid Circuitry Based On Silicon Components

Hybrid Circuitry Based On Gallium Arsenide Components

Monolithic Circuitry Using Silicon Substrates

Monolithic Circuitry Using Gallium Arsenide Substrates

Table 2. A Menu Of Technologies Available For UHF Radar Modules.

High transmit powers are more easily delivered with hybrid, rather than with monolithic, approaches

Small quantities of modules are most cost-effectively delivered from an existing hybrid facility, while larger quantities suggest a more monolithic approach

The need for gallium arsenide escalates as the frequency of operation increases

Gallium arsenide chips are more suitable than silicon circuits to radiation environments involving large potential for neutron displacement damage

Table 3. Some Technology Selection Axioms Of The High Frequency Manufacturing Community.

Potential For Low-Cost Production

Potential For Easy Testability

Potential For High Volume Scale-Up

Potential For Light Weight

Potential For Low Power Consumption

Potential For Good Performance Repeatability Among Modules

Potential For High Radiation Resistance

Potential For Long, Reliable Life

Table 4. Some Important Evaluation Criteria For Transmit/Receive Modules.

2.0 TECHNOLOGICAL VIGNETTE: THE PAVE PAWS UHF RADAR MODULES

Perhaps the most well-known, UHF phased array radar is the Phased Array Warning System (PAVE PAWS) built by Raytheon.[4-10] This radar uses solid state transmit/receive modules and operates at a frequency of 433 MHz. Identical modules have been used to upgrade the Ballistic Missile Early Warning System (BMEWS) in Thule, Greenland.

The PAVE PAWS module consists of hybrid circuitry assembled in two, nested boxes. One box contains a 4-bit phase shifter, a 2-stage low noise amplifier and a transmit/receive switch. The other box houses four, 100-watt bipolar output transistors, two drivers and a predriver. The associated matching networks employ distributed circuitry formed in microstrip. A filter is included along with circulators and a logic driver assembly. This logic driver decodes row-column commands from the beam-steering computer and, thus, eliminates the need to individually wire the computer to each module. The fully-assembled module measures 14x8x3 inches, weighs 14 pounds and butts up to a cold plate to facilitate cooling.[10]

When originally deployed, the PAVE PAWS radar modules represented a major milestone in T/R module development. However, examination of the electrical specifications in Table 5 suggests that the phase and amplitude tracking of these modules leave significant room for improvement.[4]

TRANSMIT MODE

Parameter	Specification
Frequency	433 MHz ± 13 MHz
RF Peak Power Output	284-440 Watts
RF Average Power Output	350 Watts
Pulse Width	0.25-16 mSec
Duty Cycle	0-25%
Average Efficiency	42%
Minimum Efficiency	35%
Phase Tracking Error	14° rms
Phase Settling	25° peak
Pulse Droop	0.7 dB
Harmonics	-90 dBc

RECEIVE MODE

Parameter	Specification
Gain	27dB ± 1 dB
Noise Figure	2.9 dB rms
Phase Tracking	10° rms
Number of Phase Shifter Bits	4
Phase Shifter Error	4.6° rms

Table 5. Selected Specifications For The PAVE PAWS Radar Modules. (After Hoft, Ref. 4).

3.0 SOME SOURCES OF VARIABILITY IN THE PERFORMANCE OF TRANSMIT/RECEIVE MODULES

The phased array radars of interest to this contract are desired to have low sidelobes and a high gain coefficient per unit of aperture. Consequently, very accurate control of the relative gains and phases of the radiating elements is required. Figure 3 illustrates that, while considerable progress has been made during the last quarter century, the amplitude and phase tracking of contemporary radar arrays is far from perfect. Some of this variability is a consequence of the very nature of the array environment while other contributors consist of imperfections in the T/R modules themselves.

3.1 Systems Issues

The current flowing on each of the radiating elements is partially determined by the forward and reverse waves on the transmission line connecting the T/R module to the respective antenna element. This current is further augmented by any external signals incident on that radiator. Thus, the load impedance seen by a module is comprised not only of the self-impedance of the physically-connected element, but also of the mutual impedance induced by adjacent elements. These impedances are a function of the module's physical position in the array and of the instantaneous gain and phase signatures of the surrounding modules. Consequently, identical modules will not, in fact, perform identically when they are assembled into an active, phased array.

Other systems-related sources of radar module variations are summarized in Table 6. Of particular significance is the plethora of temperature coefficients characterizing the many components in the T/R module. As the module heats and cools by various mechanisms, these temperature coefficients cause the associated components to change their performance. However, because nearly all of the temperature coefficients are different, the performance of a module with, for example, high solar loading will not mimic a similar module which is temporarily located in the shade.

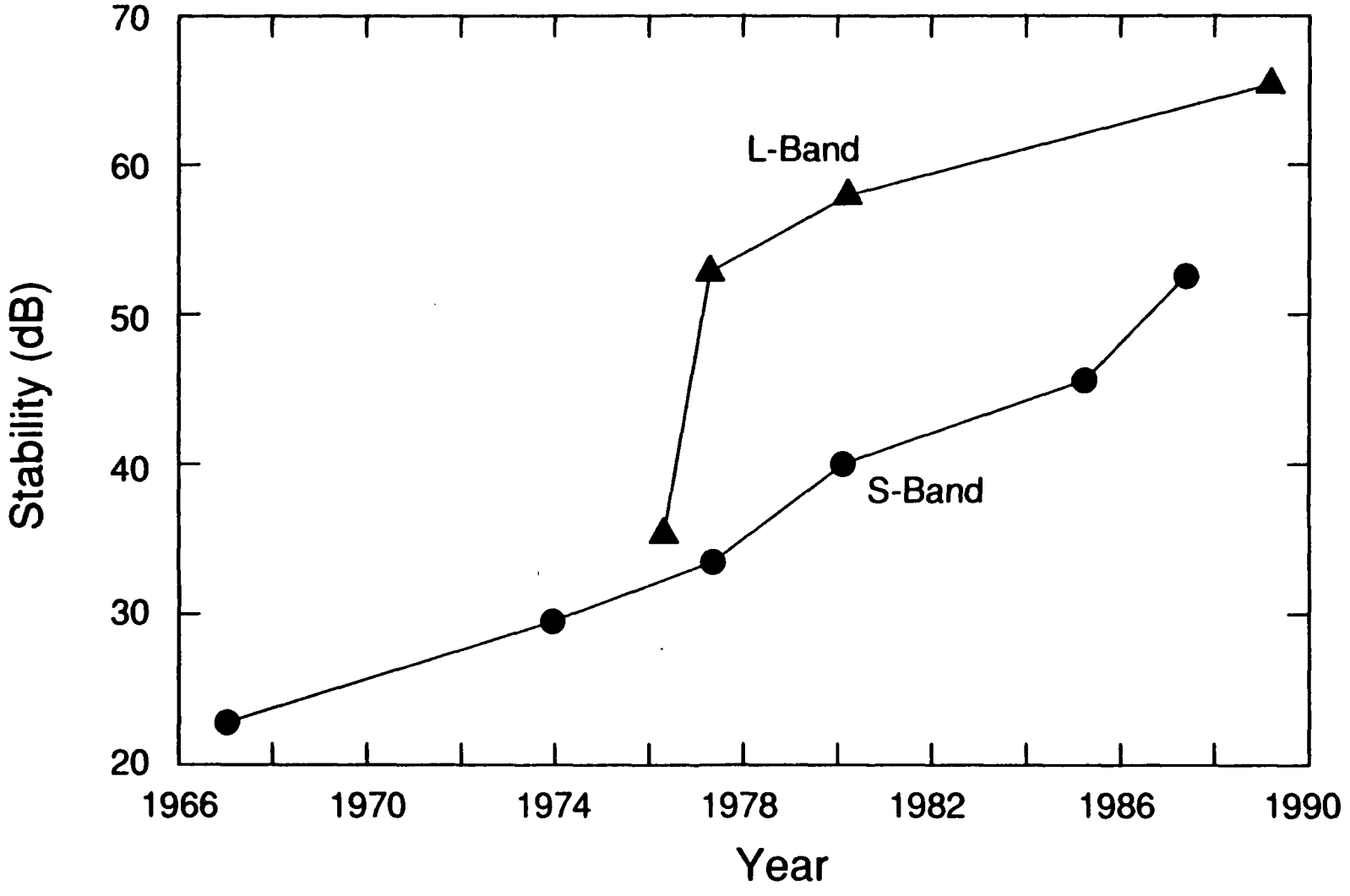

Figure 3. Typical Improvements In Radar Stability. (Data Courtesy Of Perry Sorrell, Westinghouse).

Load Mismatches Caused By Module Position Effects

Load Mismatches Caused By Frequency Scanning Effects

Load Mismatches Caused By Directional Scanning Effects

Temperature Gradients

Temperature Rise During The Transmitted Pulse

Fluctuations In Bias Voltages

Switching Transients

Module Placement Variations

Vehicle Flexure

Table 6. Some Systems-Related Sources Of Radar Module Variations.

Further complicating matters is the inevitable temperature rise during the radar pulse. This causes heating of the active semiconductor junctions with a concomitant runout of transistor gain and phase during the pulse itself.

Finally, flexure of the vehicle supporting the phased array can significantly compromise the performance of the radar system. For example, at 450 MHz, a wavelength in free space is only about 66.7 centimeters. Thus, less than two millimeters of flex in the aircraft, or other support vehicle, causes a one degree phase error in the resulting signal.

3.2 Module Issues

Aside from the systems issues discussed above, there are a number of other contributors to phase and gain variability on a module-to-module basis. These variations can be conveniently categorized into materials, passive component, active component and assembly issues as summarized in Tables 7-10, respectively. These lists, of course, are not intended to be exhaustive, but they do hint at the magnitude of the problems facing a contemporary, transmit/receive module designer. Certainly, the various temperature coefficients of the constituent components is a major issue *and* the large variation of ferrite circulator performance with temperature is particularly vexing. Conversations with industrial experts suggest that noisy frequency sources is another major contributor to module variability. Many of the frequency sources being used today resonate at fairly low fundamental frequencies. Consequently, several stages of frequency multiplication, often, are introduced in order to escalate the frequency source to the desired band. However, the noise increases by about six decibels for each doubling in frequency and this causes significant problems in real radar systems.

As enumerated in Table 10, component placement variations in hybrid modules can be a large contributor to module variability. A typical, robotic pick-and-place system might feature a placement accuracy of about ±0.010 inches. Unfortunately, 10 mils of

Doping Variations In The Gallium Arsenide Substrate

Crystal Defects In The Gallium Arsenide Substrate

Traps In The Gallium Arsenide Substrate

Doping Variations In The Silicon Substrate

Crystal Defects In The Silicon Substrate

Traps In The Silicon Substrate

Permittivity Variations In The RF Substrate

Lithography Variations On The RF Substrate

Table 7. Some Materials-Related Sources Of Radar Module Variations.

Passive Component Manufacturing Variations

Temperature Variations In Passive Component Parameters

Noise Characteristics Of Passive Components

Noisy RF Connectors

Leaky RF Connectors

Vibrating Connectors

Vibrating Waveguides

Vibrating Air Dielectric Transmission Media

Table 8. Some Passive Component-Related Sources Of Radar Module Variations.

Gain Characteristic Tolerances Of Active Components

Phase Characteristic Tolerances Of Active Components

Low Frequency Instability In Amplifiers

Frequency Tolerance Of Oscillators

Noisy Frequency Sources

Table 9. Some Active Component-Related Sources Of Radar Module Variations.

Component Placement Variations

Wire Bonding Variations

Mechanical Stress Variations On Components

Module Aging Issues

Table 10. Some Assembly-Related Sources Of Radar Module Variations.

placement inaccuracy constitute more than 1/2 degree of phase uncertainty for a 450 MHz module built on alumina.

Finally, module aging effects have been reported in the literature.[11] Presumably, non-hermetic module packaging contributes to such aging. However, the long-term, natural relaxation of epoxy die-attach materials changes the stress on their associated chips and, thus, can detrimentally modify the performance of the corresponding module.

4.0 SOME WAYS TO OBTAIN IMPROVED TRANSMIT/RECEIVE MODULES

Perusal of the literature on phased array radar modules, an examination of actual radar systems and conversations with experts in the module arena suggest that further improvements can be made in the performance of T/R modules. The general thrust of such improvements is likely to be two-fold as summarized in Table 11. Certainly, one field ripe for progress involves methods to make the modules themselves more nearly identical. Complementing these efforts will be attempts to provide improved means for the modules to adapt to their changing environment as the array is exercised in the field.

Sections 4.1 - 4.5 will discuss five general areas which Georgia Tech believes can help make future UHF modules more nearly identical. Subsequently, Sections 5.1 - 5.2 present some thoughts on techniques for providing a module with the means to adapt to its array environment.

4.1 The Use of Transistors at Lower Frequencies

There is a tendency among military systems designers to force available transistors to operate near their upper frequency limit. Such an approach encourages, for example, the use of a transistor specified for V-band operation in the design of V-band hardware. At these elevated frequencies, however, the transistor is beginning to suffer degradations in noise figure, gain and linearity. These performance handicaps tend to make the resulting electronics overly sensitive to minute fluctuations in both transistor parameters and ambient conditions.

In contrast to this approach, it may be appropriate to employ transistors whose gain-bandwidth product greatly exceeds the eventual requirement of the constituent system.[12,13] The transistors themselves will perform better when not pushed to their ultimate limit. An example of such a performance improvement can be seen in Figure 4. This figure plots the noise figure of a high performance, high electron mobility transistor (HEMT) as a function of operating frequency. Note that at V-band, for instance, the

Fabricate More Nearly Identical Modules

Provide Improved Ways For The Modules
To Adapt To The Array Environment

Table 11. The Two Basic Ways To Improve The Performance Of Phased Array Radar Modules.

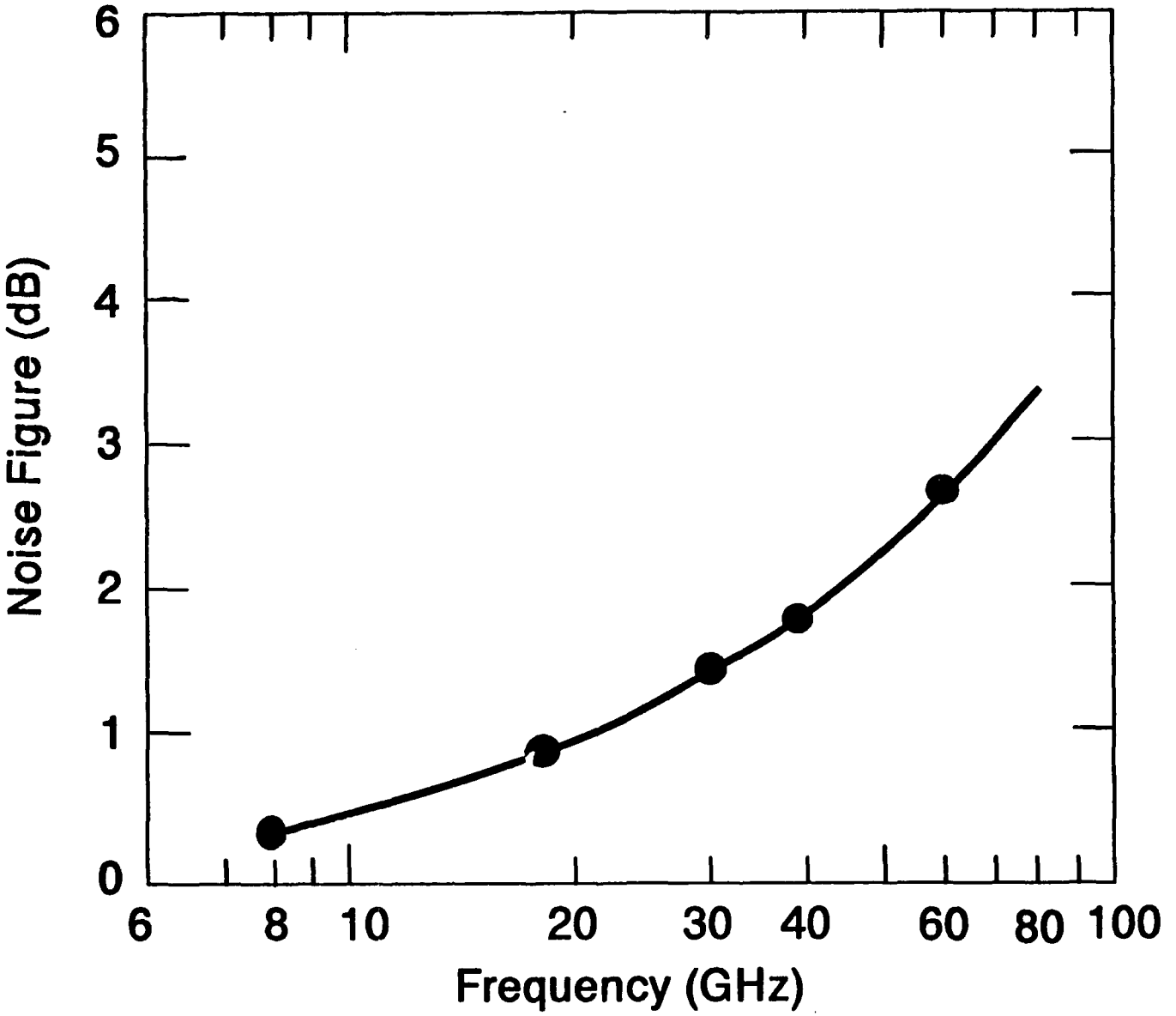

Figure 4. Noise Figure Performance Of A High Electron Mobility Transistor. (Data Courtesy Of General Electric).

transistor features a typical noise figure of about 2.7 decibels. However, if the same V-band device is allowed to operate at X-band, the resulting noise figure is only a small fraction of a decibel. Table 12 illustrates that a similar improvement in gain can be achieved by permitting the transistor to operate well below the upper end of its frequency performance envelope. In this case, the HEMT displays only 4.4 dB of gain at V-band, but enjoys a gain of 12-15 dB at X-band.

A further advantage of operating transistors below their ultimate frequency limit is that the excess gain-bandwidth can be traded-off in an attempt to improve other parameters of the overall circuit. A trade-off well worth considering is the use of negative feedback to improve the linearity performance of an amplifier or to provide for automatic gain control for a receiver system. These, and similar, active feedback approaches are discussed in detail in Section 5.2.

As an illustration of the value of using transistors well below their upper frequency limit, Georgia Tech researchers designed a UHF amplifier around X-band gallium arsenide (GaAs) transistors. These transistors were fabricated at Georgia Tech using a conventional metal-semiconductor field effect transistor (MESFET) process and were originally constructed for operation at X-band.[14] For purposes of this demonstration, however, they were used in the design of an amplifier intended to operate between 20 MHz and 1 GHz and intended to have more than 40 dB of gain over this entire frequency band. A further intention of the exercise was the elimination of the large-area inductors normally employed in the associated matching networks. This was done by recognizing that a common-gate MESFET displays an impedance approximately equal to the reciprocal of its transconductance. Clearly, the layout geometry of such transistors can be adjusted such that this corresponding impedance is, for example, equal to 50 ohms. Figure 5 illustrates the employment of these matching networks for both the input and the output ports of the UHF amplifier. A schematic of the complete circuit appears in Figure 6. Note that the circuit employs no inductors and that it makes extensive use of the primary

Operating Frequency (GHz)	Transistor gain (dB)
8	15.2
12	12.5
18	10.4
30	10.0
40	7.5
62	4.4

Table 12. Gain Performance Of A High Electron Mobility Transistor. (Data Courtesy Of General Electric).

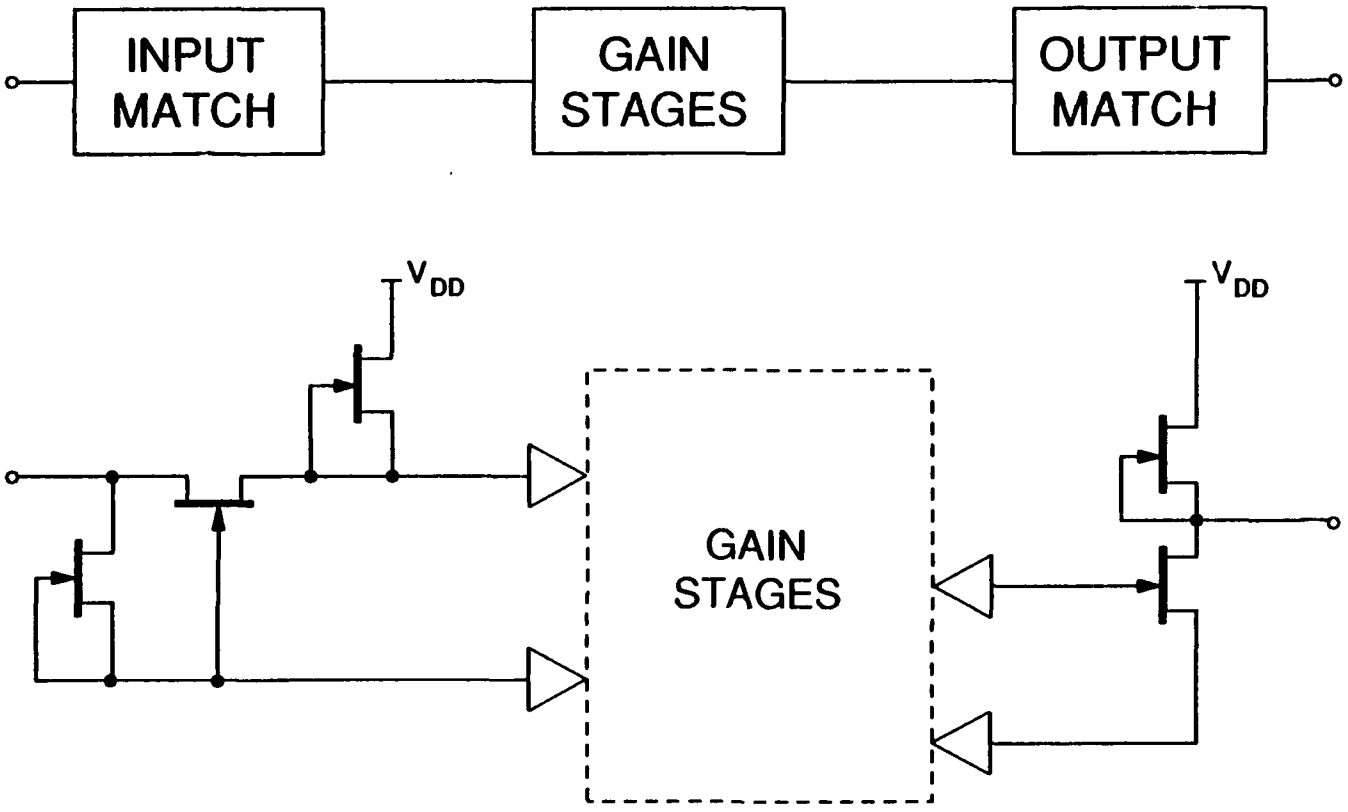

Figure 5. Simplified Schematic For An Improved UHF Amplifier. (Courtesy Of R.K. Feeney And D.R. Hertling, Georgia Tech).

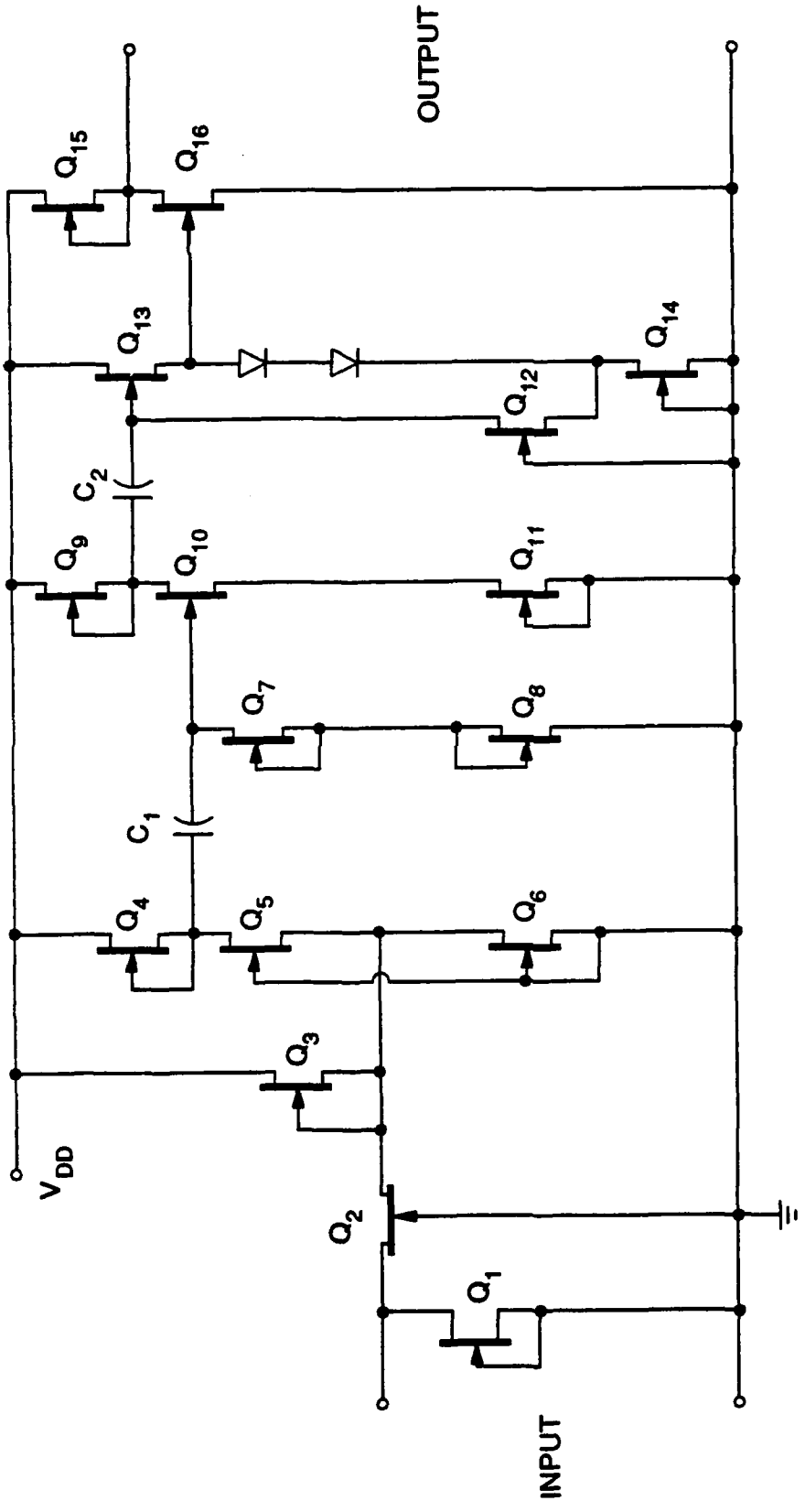

Figure 6. Complete Schematic For The UHF Amplifier. (Courtesy Of R.K. Feeney And D.R. Hertling, Georgia Tech).

active device. Figure 7 shows the gain response of the complete amplifier. It is apparent that the design goals have been met and that exemplary UHF performance can be achieved with the appropriate transistors. It is further emphasized that the MESFET devices used extensively in this design occupy considerably less chip area than that required by spiral inductors and distributed matching networks. In fact, the chip size of the Georgia Tech amplifier is only about 1/5 that of a similar circuit made with a more conventional approach. Consequently, the same wafer can accommodate about five times as many potential amplifiers.

4.2 The Use of Balanced Circuitry

Many of the high frequency circuits being designed today use an active device biased for Class A operation. Figure 8 illustrates a Class A bias configuration for a bipolar transistor. It is well-known that an envelope defined by cutoff, saturation and the appropriate breakdown voltage defines the maximum dynamic range available from the transistor in this configuration.

A way of doubling the dynamic range of such an arrangement is by adding an identical transistor and several transformers to the circuit as illustrated in Figure 9. In this case, the bias point advocated in Figure 10 may be employed. It is apparent that the symmetry inherent in this situation provides the capability of operating a balanced, Class B circuit. When using Class B, the even harmonic products are cancelled by the identical transistors operating in opposition. Of course, any non-linearities in the transistors still produce odd harmonics. In fact, with bipolar devices, because of an inherent non-linearity in the base current versus base-to-emitter voltage characteristic, the load current will be distorted near the zero crossings. Such a phenomenon is conventionally referred to as "crossover distortion." In contrast, field effect transistors (FETs) have a square-law transfer characteristic. Consequently, an analogous circuit using FETs will produce no odd harmonics and, thus, is essentially distortion free.

Now, consider the case where complementary devices are available, each having more gain than that required to operate

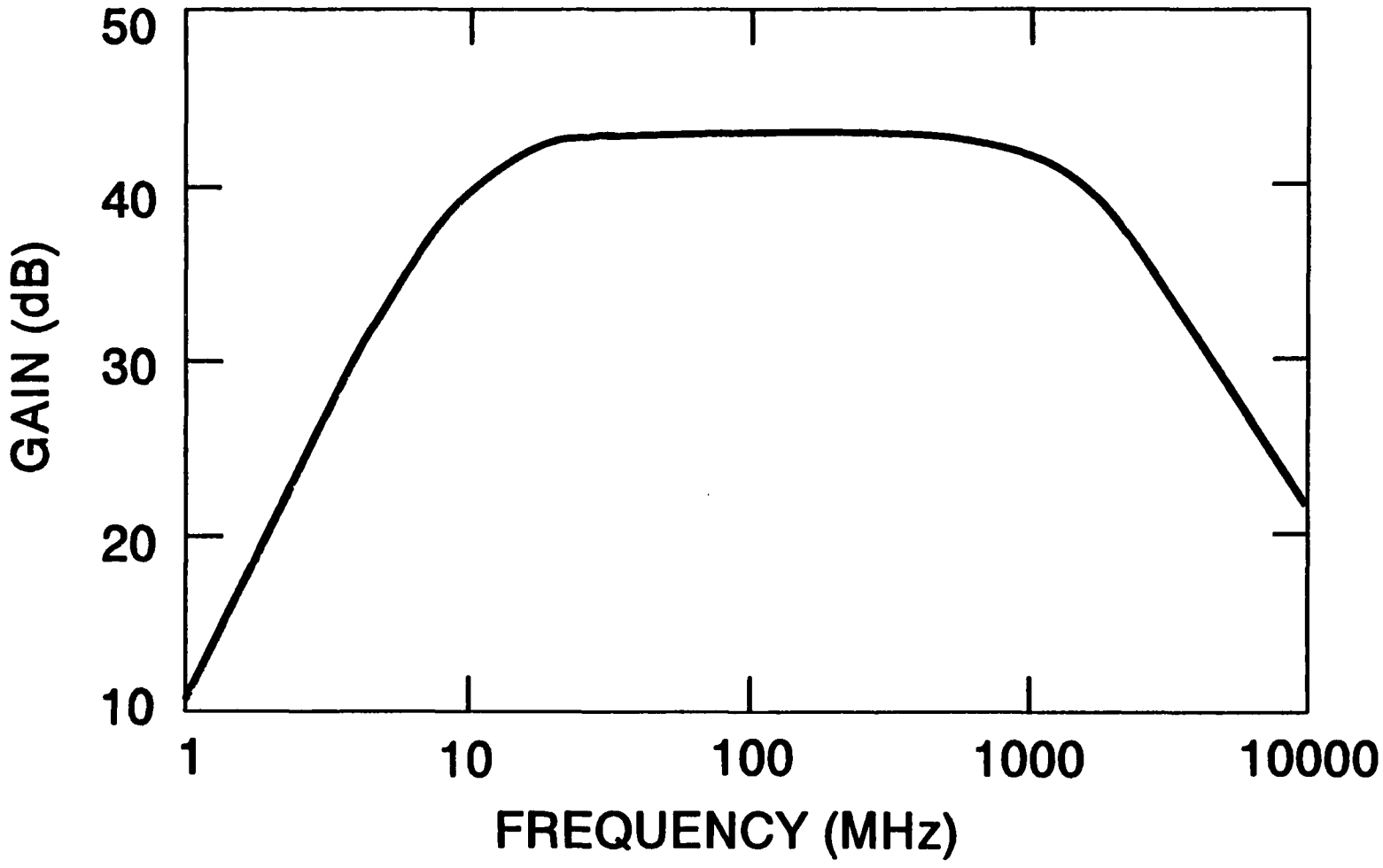

Figure 7. Gain Response Of The UHF Amplifier.
(Courtesy Of R.K. Feeney And D.R. Hertling, Georgia Tech).

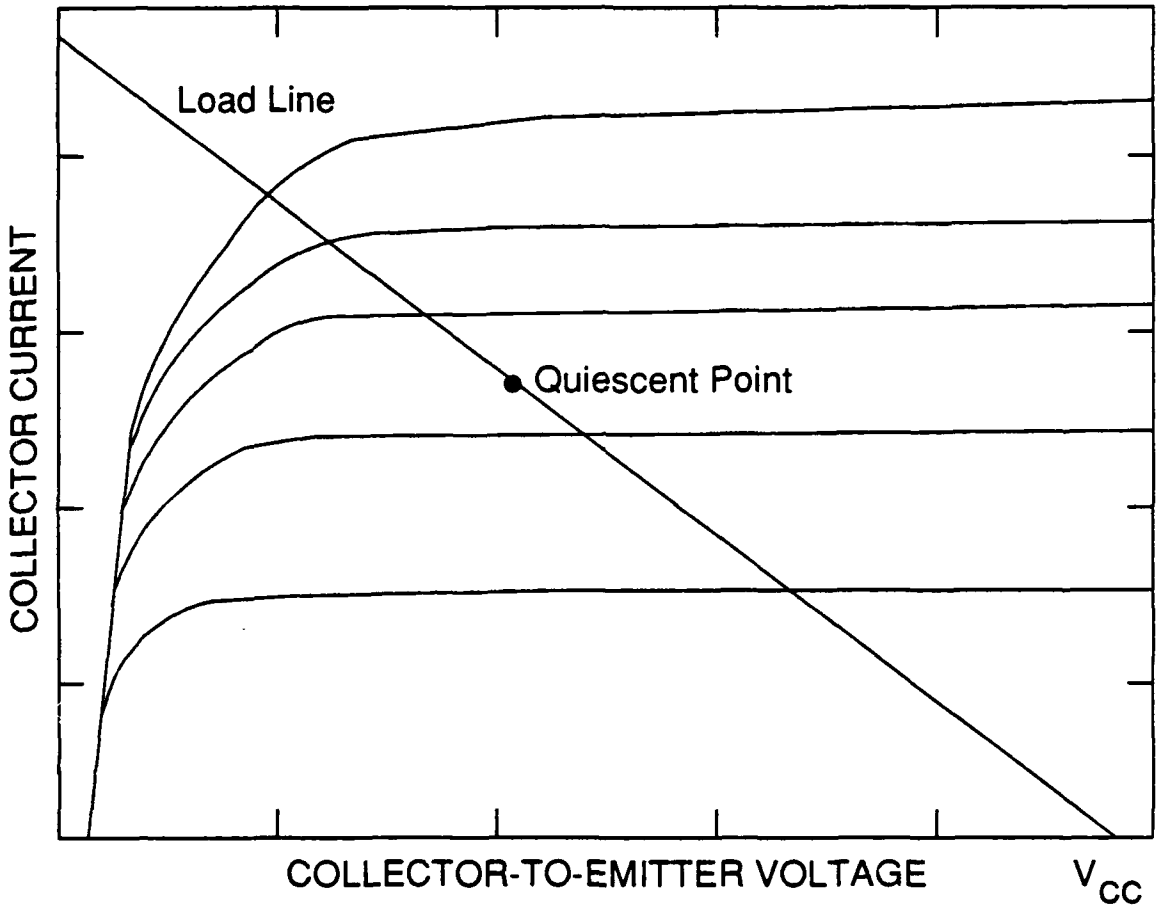

Figure 8. A Bipolar Transistor Biased For Class A Operation.

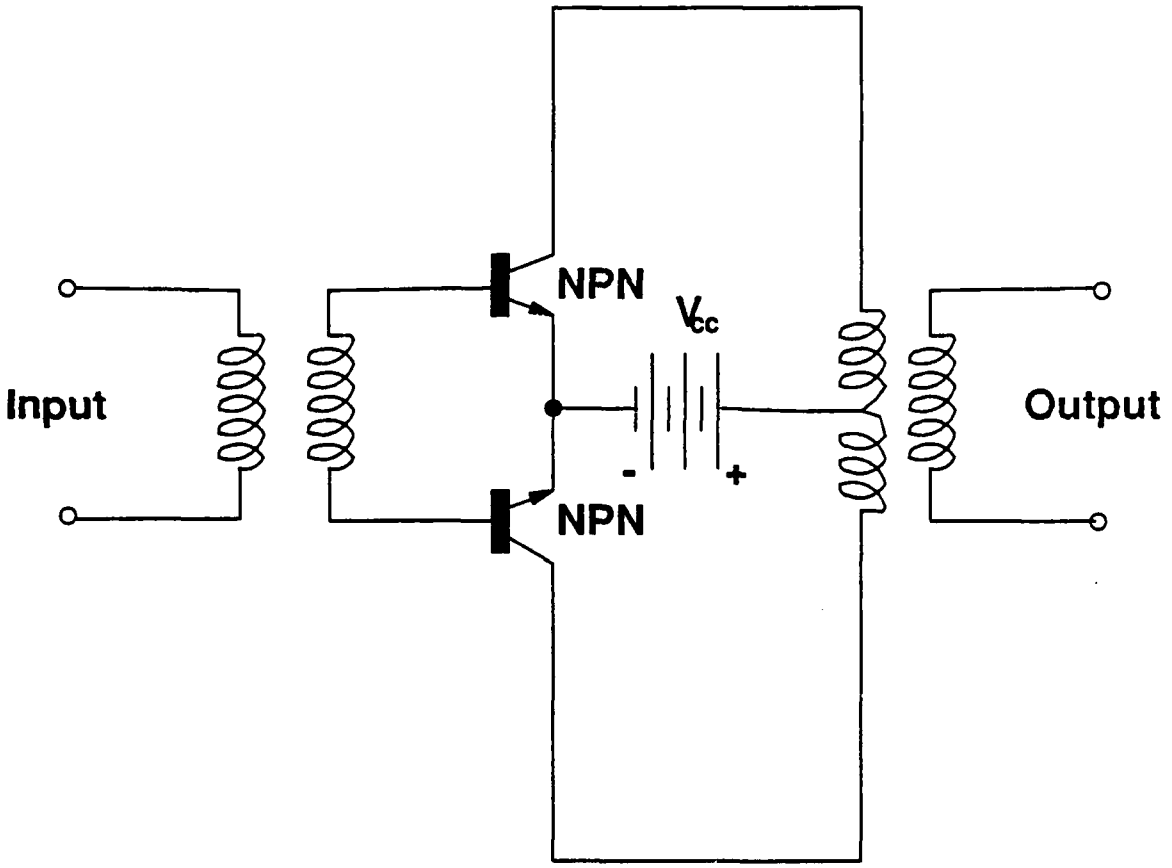

Figure 9. An Example Of Balanced Circuitry Using NPN Transistors. (Courtesy Of D.R. Hertling, Georgia Tech).

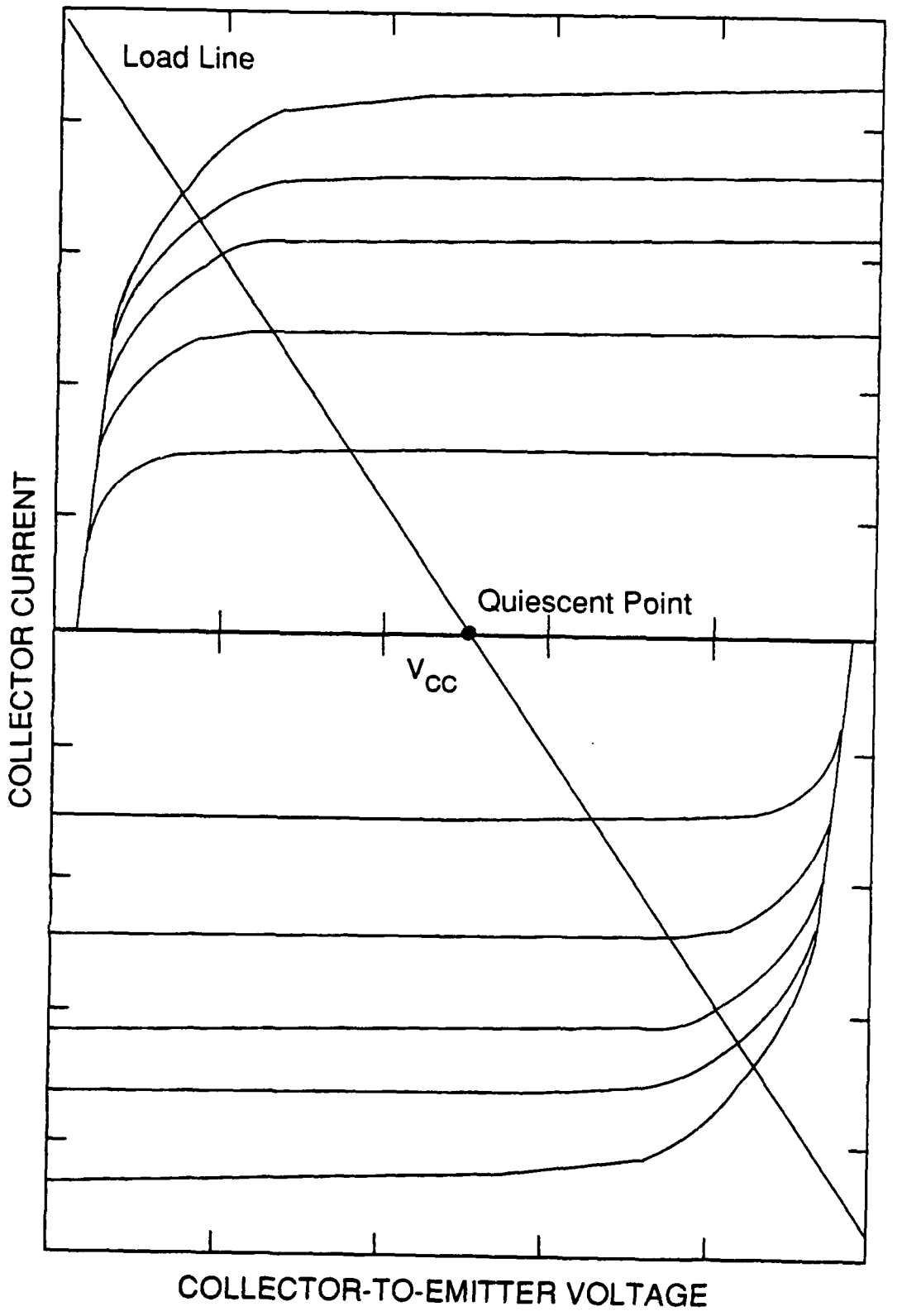

Figure 10. A Balanced, Bipolar Circuit Biased For Class B Operation. (Courtesy Of D.R. Hertling, Georgia Tech).

Class A.[10] In this event, they may be hooked up in a balanced configuration, as shown in Figure 11, without the necessity of auxiliary transformers. As in the case with non-complementary devices, proper selection of the quiescent point can double the dynamic range of the circuit. Furthermore, with perfectly-matched transistors, the even harmonics are eliminated altogether.

Unfortunately, the extensive utilization of balanced circuitry is discouraged in the higher frequency world by the unbalanced, 50 ohm heritage of the conventional microwave community. In fact, the design of the majority of test equipment, antennas and similar hardware has, essentially, forced the continued proliferation of unbalanced, 50 ohm designs. Recognizing this, M. N. Yoder has pointed out that "the 50 ohm, unbalanced interface (is) an unnecessary and performance-limiting carryover from a bygone era."[15] He further argues that future, high frequency integrated circuits could be significantly improved if the systems designers would simply specify a balanced interface. In the meantime, some sort of a balanced-to-unbalanced converter seems appropriate.

Moreover, it is interesting to note the insistence on 50 ohm interfaces at the inputs and outputs of every stage on a complex chip. Apparently this is a consequence of each building block being designed separately, tested on conventional, 50 ohm equipment and, then, monolithically located to make the integrated circuit desired in the first place. Clearly, there is no reason for all of these intermediate nodes to be perfectly matched to 50 ohms. The only place a 50 ohm interface is required is on the outside of the housing itself. It seems appropriate to consider making the internal impedances whatever values are necessary to enhance the performance of the overall system. Of course, as a practical matter, it is hard to get either extremely low or extremely high impedances in high frequency hardware. However, values from, perhaps, several ohms to several thousand ohms are readily achievable and provide considerable flexibility to designers no longer forced to match every node to 50 ohms.

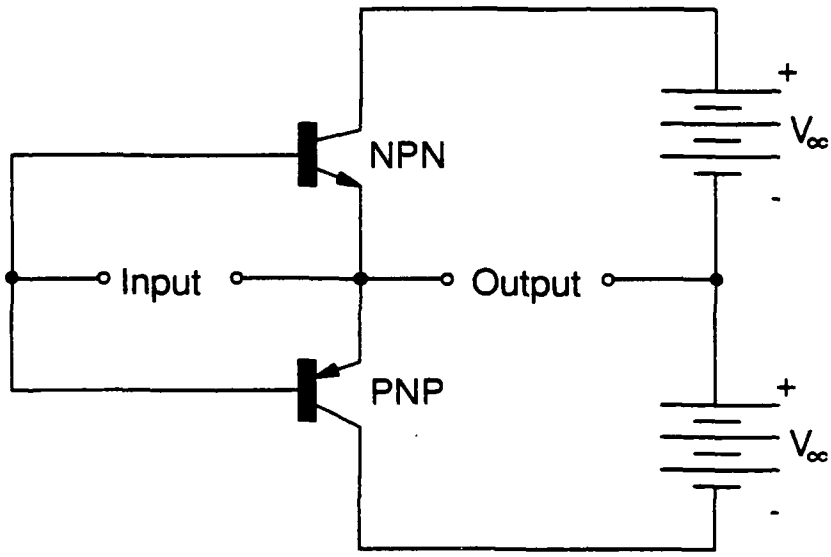

Figure 11. An Example Of Balanced Circuitry Using Complementary Transistors. (Courtesy Of D.R. Hertling, Georgia Tech).

4.3 Improved Power Devices

4.3.1 Introduction

An area of ongoing concern for T/R modules involves the limitations of available power devices. Electron tubes have seen extensive use in UHF radars while, more recently, solid state elements have become popular. Clearly, the transmitter function requires the selection of an appropriate power device. However, as will be shown, the receiver might also benefit from the insertion of devices with improved power handling capabilities.

4.3.1.1 Transmitter Issues

For transmitter applications, the requisite power devices, above all else, need to be capable of delivering the required power to the antenna structure. Historically, electron tubes have been widely used in radar systems. Tubes still are a good bet when exceedingly-high transmit powers are required. Unfortunately, tubes have a number of significant drawbacks as enumerated in Table 13. Fortunately, several of the serious disadvantages of tubes can be overcome with contemporary solid state components. Furthermore, the extensive research being carried out in the general area of microelectronics suggests that future performance enhancements will, most likely, be realized in the solid state arena rather than with conventional electron tubes.

It is, of course, well-known that there tends to be an inverse relationship between the output power available from a device and its frequency of operation. Figure 12 illustrates a manifestation of this phenomenon for typical, silicon bipolar transistors. Similar performance degradation with increasing frequency has been observed for metal-oxide-semiconductor field effect transistors (MOSFETs). Upon examining commercially-available devices from each category, Georgia Tech believes that either bipolar or MOS transistors are suitable for very high frequency (VHF) applications. However, for systems with very high duty factors, one might consider favoring the MOSFETs. In contrast, at UHF, the available silicon bipolar transistors seem to have the edge at the present time.

Advantages	Disadvantages
Deliver very high power	Higher weight than a solid state radar
High dynamic range	Susceptible to vibration
May result in a lower acquisition cost than a solid state radar	Higher maintenance cost than a solid state radar
	Tend to degrade catastrophically
	Have a finite shelf life
	Few tube experts are entering the workforce
	Do not seem to be the wave of the future

Table 13. Selected Characteristics Of Conventional Electron Tubes.

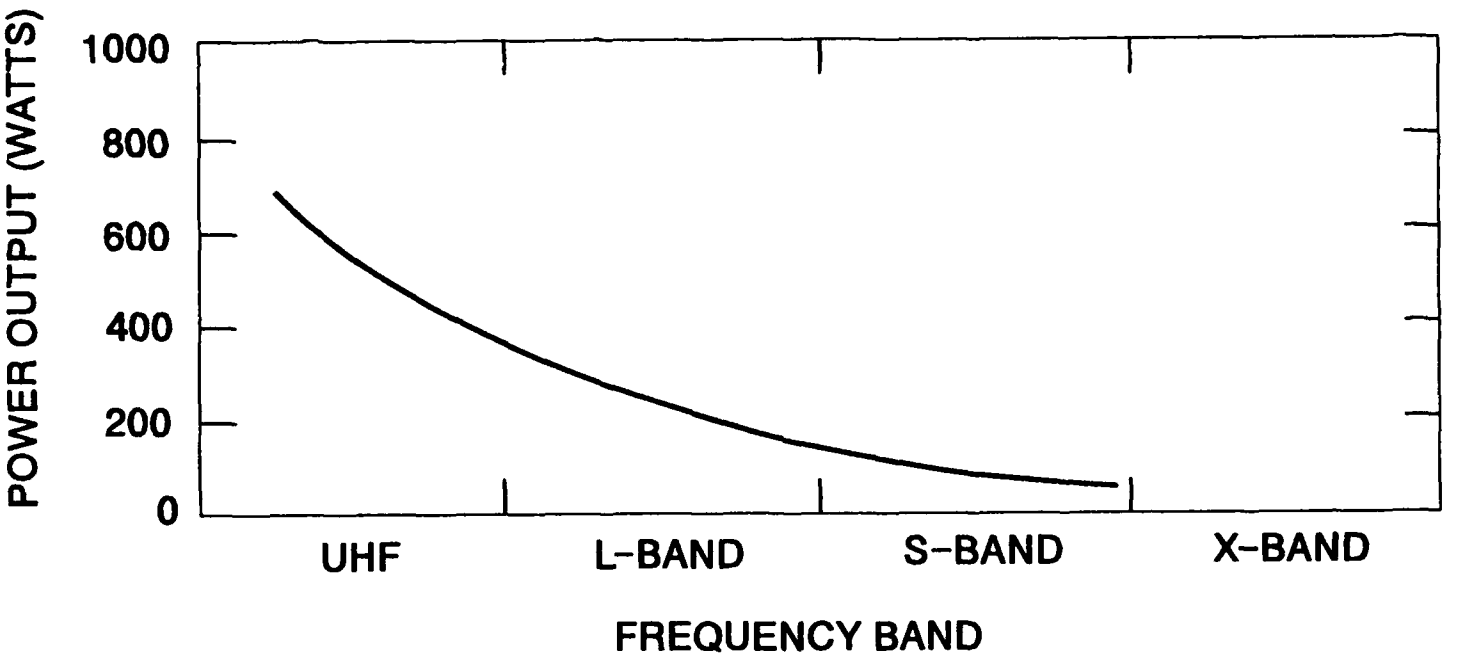

Figure 12. Typical Output Power Available From Silicon Bipolar Transistors. (Data Courtesy Of Ken Petrosky, Westinghouse).

4.3.1.2 Receiver Issues

An important figure of merit for a receiver is its dynamic range. The dynamic range is a function of the receiver's linearity and a high dynamic range results in a receiver less susceptible to intermodulation distortion. There are a number of ways of increasing the dynamic range of a receiver and a few of these techniques are summarized in Table 14.

The dynamic range of most receiver systems is limited by the corresponding dynamic range of the active elements. Consider, for example, the transistor characteristics of the field effect device illustrated in Figure 13. Notice that the maximum signal swing is limited by the drain saturation current (I_{DSS}) on one side and the drain-to-source breakdown voltage (BV_{DS}) on the other.[10] Clearly, increasing the size of this envelope escalates the dynamic range available from the FET. Another way of stating this is to observe that an active device with lots of power handling capability can be used to increase the dynamic range of its host receiver.

4.3.2 Electron Tubes

Tubes totally dominated the radar market during the first three decades of its existence and only began to surrender this position to solid state devices in the mid-1970s. An unfortunate characteristic of the architecture of tube-based systems is that only one, or several, tubes support the entire radar array. Consequently, failure of just a single tube results in catastrophic degradation of the array. In contrast, solid state proponents tend to distribute their high power transistors in many T/R modules. Therefore, a transistor failure results only in the, so-called, "graceful degradation" of the array. An additional advantage of the distributed module approach is that it permits phase shifting to occur prior to power amplification. Thus, phase shifter losses are less problematic and, in any event, can be compensated for by the subsequent amplifier. In essence, the trend in contemporary module design is to generate power as close to the antenna element

Decrease The Bandwidth

Increase The Power Handling Capability

Increase The Linearity

Decrease The Sensitivity

Use Negative Feedback

Table 14. Some Ways Of Increasing The Dynamic Range Of A Receiver.

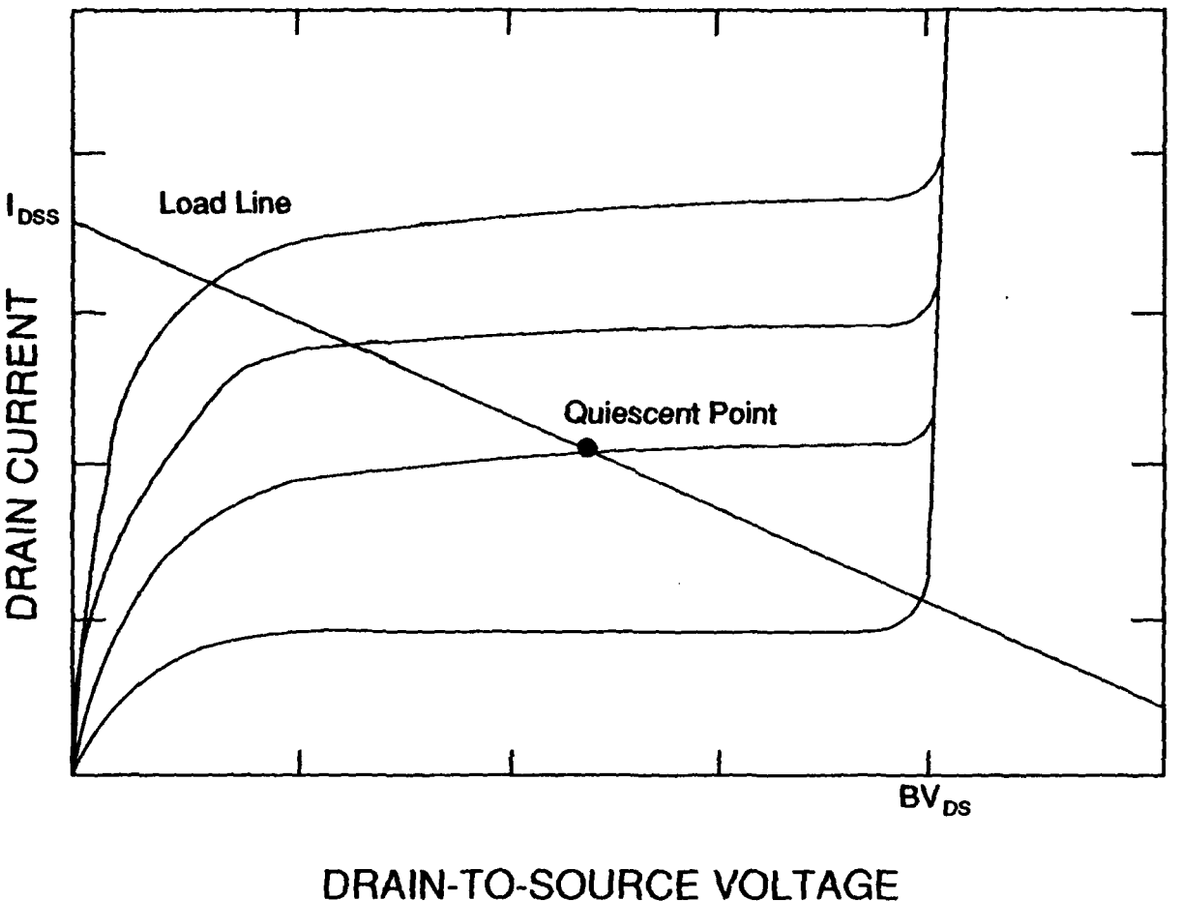

Figure 13. A Field Effect Transistor Biased For Class A Operation.

as possible.[10] Clearly, tube-based systems make it difficult to conform to this adage.

Table 13 reviews a number of the characteristics of electron tubes. A particularly serious handicap is that conventional tubes have fallen out of favor with the designers of all but the very highest power radar systems. Moreover, the older, tube experts are leaving the workforce and most young engineers have no formal education with tubes.

A distant grandchild to the vacuum tube is beginning to surface and exists under the general guise of a vacuum microelectronic device.[16] Such an element is built using semiconductor-like processing and is, as seen in Figure 14, a tiny tube fabricated in a substrate. This device features a very fast carrier transit time which translates to a high operating frequency. Furthermore, because it is a vacuum tube-like item, it may enjoy an impressive dynamic operating range. Although it is too early to give a complete prognosis for vacuum microelectronics, Georgia Tech believes it appropriate for UHF radar designers to keep a finger on the pulse of this technology.

4.3.3 Solid State Devices

4.3.3.1 Introduction

A number of solid state devices are worth consideration by the UHF radar engineer. Certainly, bipolar transistors are widely-available for operation at UHF and their continued proliferation seems assured. However, high frequency MOSFETs, static induction transistors (SITs) and solid state triodes (SSTs) are beginning to make inroads into the high frequency regime.

One reason for the intense efforts in the solid state device arena is the continued pressure to reduce the cost of the UHF transistors. Conversations with industrial radar module fabricators suggest that, perhaps, 60% of the cost of building the transmitter function results from power transistor procurement. Clearly, methods for reducing this cost handicap should be vigorously pursued. Unfortunately, a major contributor to the transistor cost lies in the price of the package itself.[17] At present, a Japanese

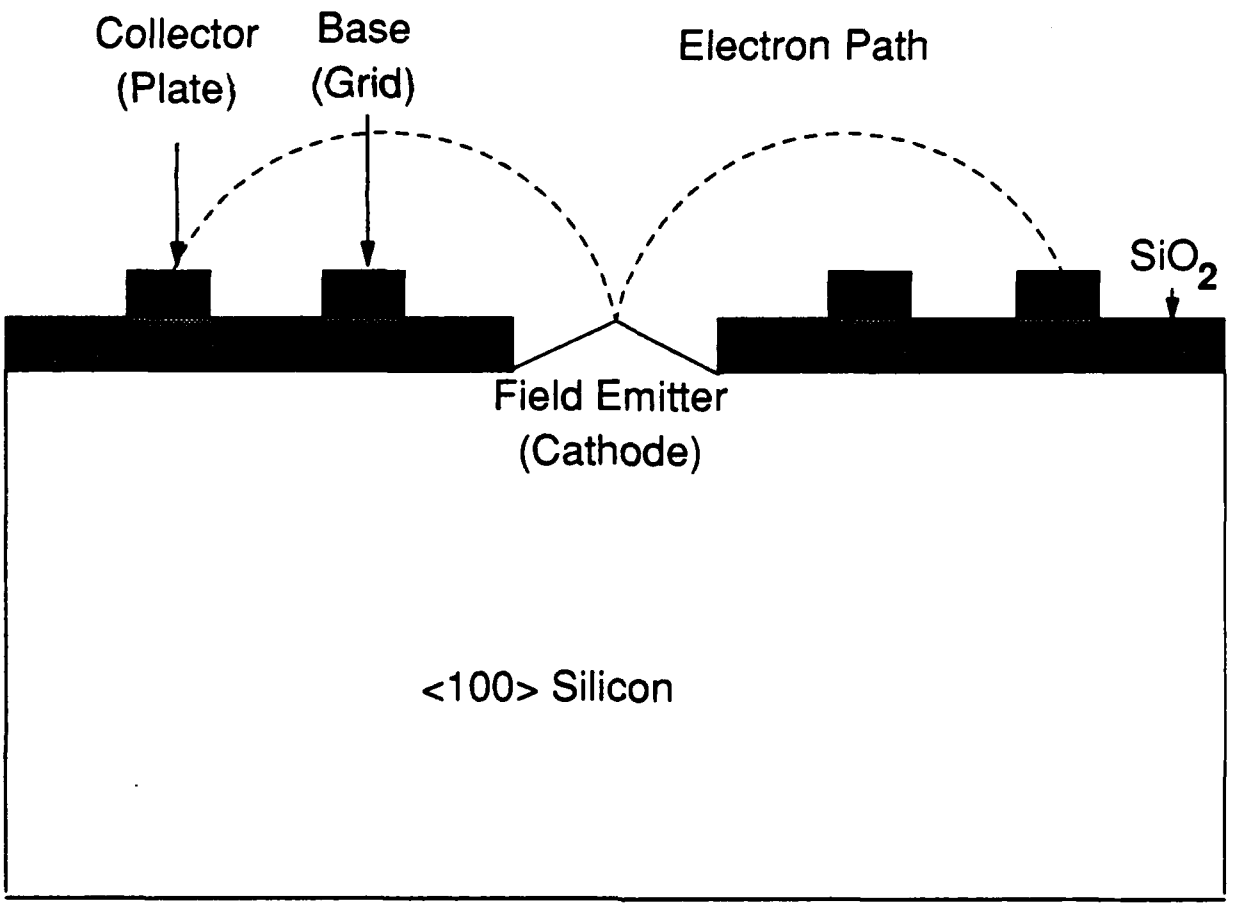

Figure 14. Simplified Cross Section Of A Semiconductor, Vacuum Triode.

company named Kyocera totally dominates the high frequency package market. It would seem attractive if an American vendor began to second-source the packages most critical for military systems.

The commercial market for UHF transistors seems to be expanding at an unprecidented rate.[17,18] The corresponding transistors are being deployed for mobile, satellite applications, position locating instruments, communications and medical electronics.[17] Presumably, the technological advances made as a consequence of these commercial uses will have some value to the military. However, a significant fraction of the commercial devices are designed to operate with either a 12½ volt or 7½ volt power supply. Thus, the ease with which this commercial technology can be applied to military systems is yet to be determined.

Finally, the power device engineer must make a fundamental decision regarding the type of semiconductor substrate that will be specified. Silicon handles UHF nicely, although, historically, there has been some tendency to lean toward gallium arsenide as the microwave band is approached. Based on the maturity of the wafer processing technology and, also, the impressive performance achieved to date, Georgia Tech recommends that silicon be considered for any system being developed for operation up through about 3-4 GHz.

4.3.3.2 Bipolar Transistors

Bipolar power transistors are the workhorse of contemporary, solid state radar modules. These transistors provide an attractive output power per unit cost and are widely available from a number of domestic suppliers. At present, bipolar transistors are the only commercially-produced, solid state devices which have reasonable performance at 450 MHz and above.

Table 15 summarizes a number of characteristics of bipolar devices. One problem with such transistors is the exponential relationship between the collector current and the base-to-emitter voltage. This dependence tends to limit the dynamic range of practical, bipolar transistors.

Susceptible to both thermal runaway and second breakdown

Higher-order intermodulation distortion is a function of both the type and the value of the emitter-ballasting resistors

Input impedance is a function of input drive voltage

Suffers from both shot noise and thermal noise

Currently, the only UHF solid state device that is widely available

Table 15. Selected Characteristics Of Bipolar Transistors.

Another feature of bipolar devices is the requirement to ballast the emitter array with small resistors in order to prevent localized thermal runaway. Unfortunately, a large fraction of the nonlinear feedback in bipolars is delivered back to the emitters through these ballast resistors.[19] Consequently, the requisite emitter ballasting tends to degrade the distortion characteristics of the transistor.

Finally, the base impedance of bipolar devices is inherently low and this is particularly true at UHF. Hence, before power combining bipolars, it is necessary to transform each base impedance to a higher level in order to facilitate the design of the combiner matching networks.[19]

4.3.3.3 Metal-Oxide-Semiconductor Field Effect Transistors

N-channel, metal-oxide-semiconductor field effect transistors (MOSFETs) transistors for power applications are, typically, fabricated using the vertical arrangement illustrated in Figure 15. A positive voltage applied to the gate tends to invert the surface of the P-wells and, thus, allows conduction between the source and the drain. Notice that the drain contact is on the back of the wafer and, as a result, the current ultimately flows vertically through the substrate. Adjustment of the substrate doping and thickness permits tailoring the drain-to-source breakdown voltage of the device. Furthermore, because an important portion of the conduction path is in the bulk of the crystal, the vertical MOS transistor is less sensitive to surface-charge problems than a more conventional, lateral MOSFET.

Although the power MOSFET is a majority carrier, enhancement mode device, there are certain analogies to the bipolar transistor as elucidated in Table 16. In contrast, some of the characteristics pecular to MOS are summarized in Table 17.[20]

One significant feature of the MOSFET is that there is a square-law dependence between the drain current and the gate-to-source voltage. Consequently, it is possible for a properly-designed MOS device to have a higher dynamic range than a bipolar

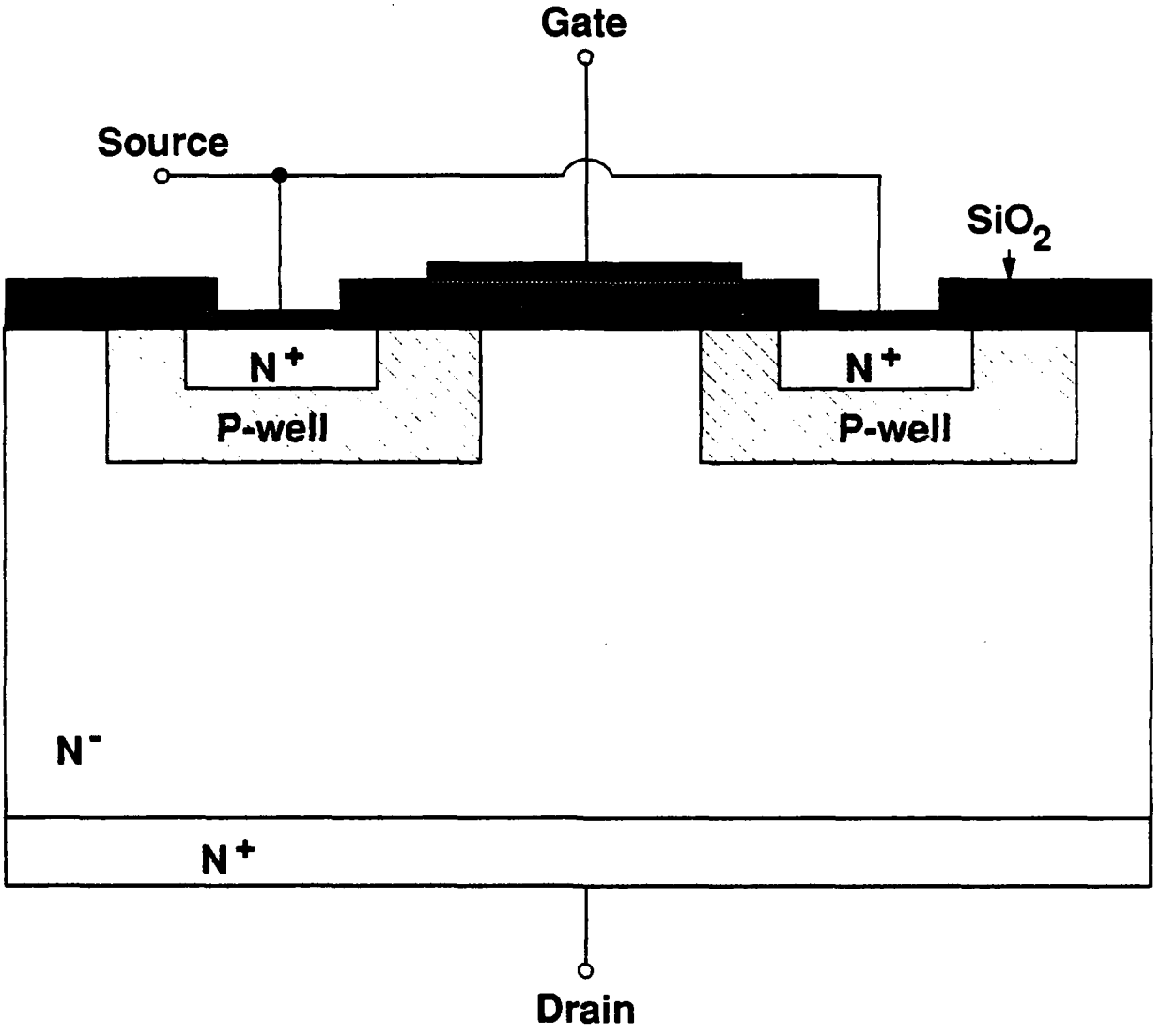

Figure 15. Simplified Cross Section Of A Power MOS Transistor.

Bipolar Nomenclature	MOS Analog
Collector	Drain
Emitter	Source
Base	Gate
BV_{CES}	BV_{DSS}
BV_{CBO}	BV_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
V_{BE} (on)	V_{GS} (threshold)
V_{CE} (saturation)	V_{DS} (on)
R_{CE} (saturation)	R_{DS} (on)
h_{fe}	g_{fs}

Table 16. Some Analogies Between Bipolar And MOS Nomenclature.

Can be biased Class A without fear of thermal runaway

Higher-order intermodulation distortion is better than with bipolars.

Lower-order intermodulation distortion is worse than with bipolars.

Input impedance is fairly insensitive to input drive voltage

Input terminal has very high impedance and, thus, must be de-Q'd with a shunt resistance or negative feedback

Displays no shot noise

Easier than bipolar to broadband

Requires a higher idling current than with bipolars

Requires more chip area than bipolar to get equal output power

May be readily used in switchmode power amplifiers.

Table 17. Selected Characteristics Of Power MOS Transistors.

transistor. It is also interesting to note that the high gate impedance of MOSFETs tends to remain capacitive to fairly high frequencies. Therefore, it is possible to power combine such FETs without the use of ancillary matching networks.[19]

A few manufacturers have begun to build vertical MOS structures which can operate well into the UHF band. Table 18 summarizes some important performance parameters of several such transistors. Note, in particular, that low noise figures have been achieved for even the high power devices. Presumably, continuing advances will result in even better performance in the future. Consequently, it is interesting to ponder the considerable advantages of using an appropriate, high power MOSFET in the front end of a solid state receiver.

4.3.3.4 Static Induction Transistors (SITs)

The static induction transistor is a vertical, field effect device as shown in Figure 16. However, unlike the vertical MOSFET, the current conducted by the SIT is a strong function of both the gate and the drain potentials.[21] Consequently, a varying drain bias changes the output current, even in the presence of a fixed gate voltage. This leads to vacuum tube-like transfer characteristics as shown in Figure 17.

The static induction transistor is a high voltage device and, thus, derives its power handling capability via an elevated breakdown voltage rather than by an ability to conduct extreme values of current.[17] Previous research has suggested that the SIT may enjoy reasonable noise performance because the channel region is buried in the substrate and, therefore, removed from the relatively more defective surface region.[22] In any event, there are no minority charge storage problems because the SIT is a voltage-controlled, majority carrier device. Consequently, the static induction transistor can operate at high frequencies and high power performance into the UHF range has been reported.[21]

Part Number	Output Power (Watts)	Frequency Of Operation (Megahertz)	Noise Figure
MRF 134	5	2-400	2.0 dB @ 150 MHz and 0.2 amperes
MRF 161	5	2-400	3.0 dB @ 400 MHz and 0.1 amperes
MRF 136	15	2-400	1.0 dB @ 150 MHz and 0.5 amperes
MRF 162	15	2-400	2.0 dB @ 400 MHz and 0.3 amperes
MRF 163	25	2-400	2.5 dB @ 400 MHz and 0.5 amperes
MRF 137	30	2-400	1.5 dB @ 150 MHz and 1.0 amperes
MRF 171	45	2-200	1.5 dB @ 150 MHz and 1.0 amperes
MRF 172	80	2-200	1.5 dB @ 150 MHz and 2.0 amperes
MRF 174	125	2-200	3.0 dB @ 150 MHz and 2.0 amperes

Table 18. Some Performance Parameters Of Selected, High Frequency, Power MOS Transistors. (Data Courtesy Of Motorola).

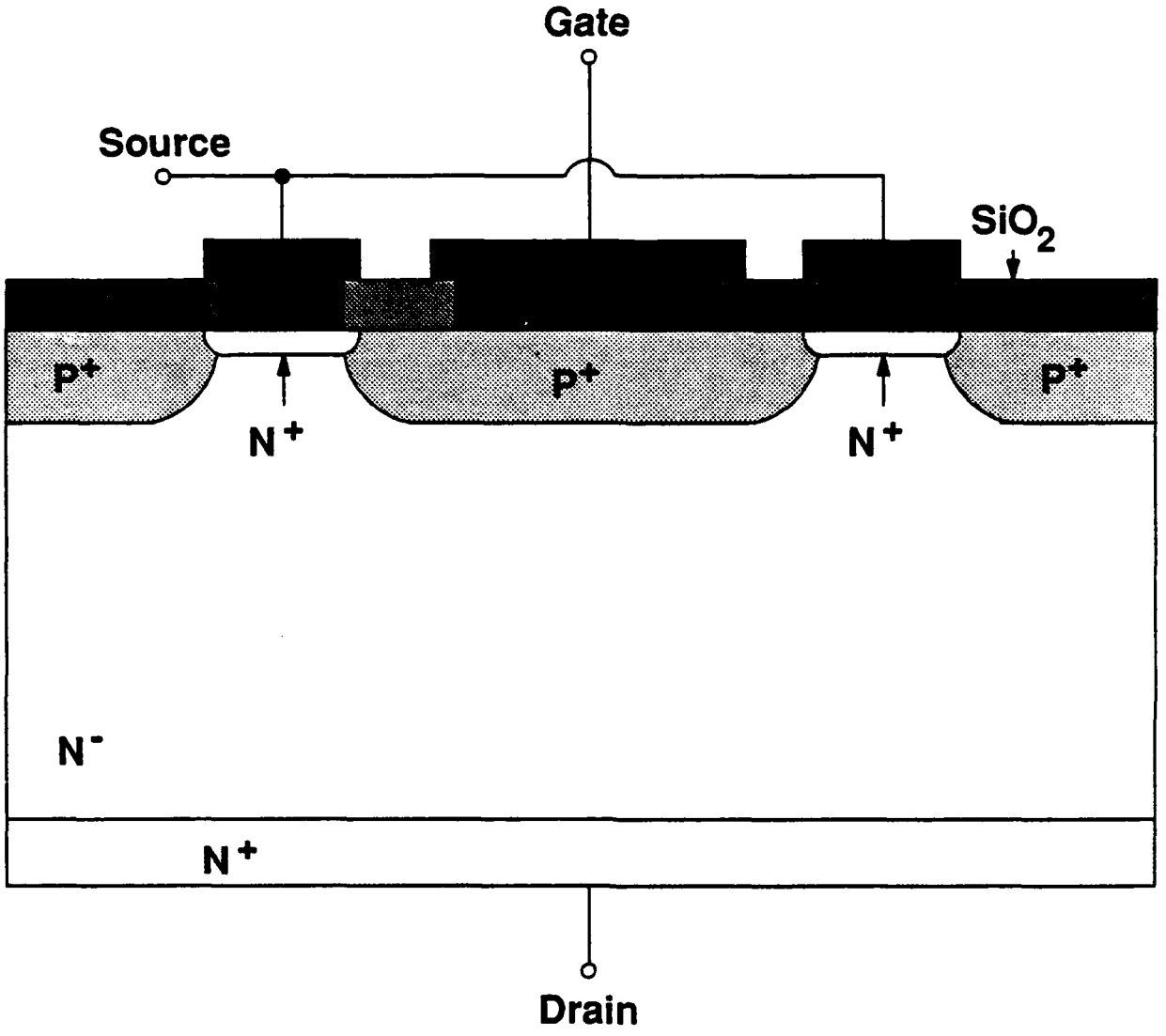

Figure 16. Simplified Cross Section Of A Static Induction Transistor.

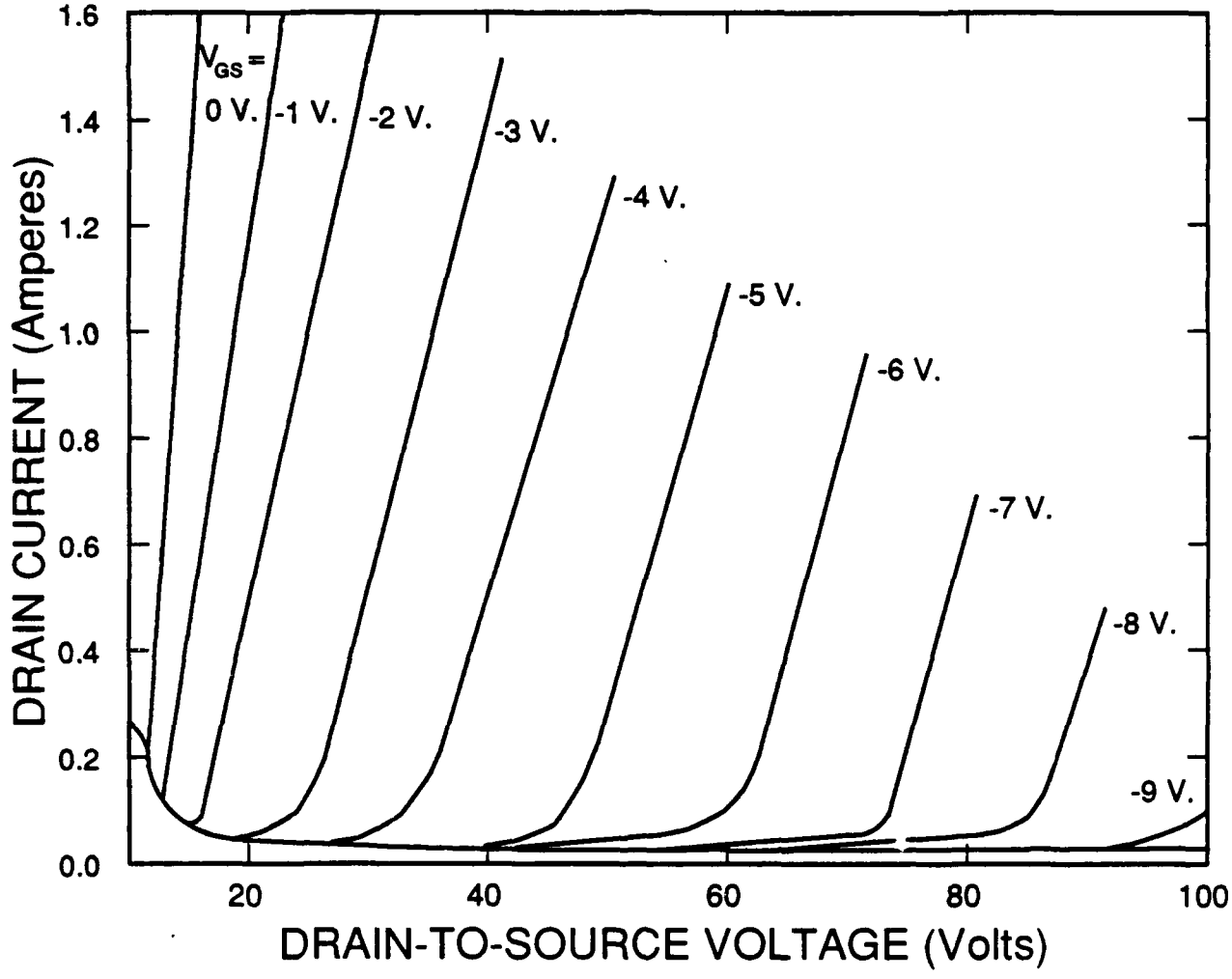

Figure 17. Current Versus Voltage Characteristics For A Static Induction Transistor.

4.3.3.5 Solid State Triodes (SSTs)

A variation of the static induction transistor is illustrated in Figure 18 and is being commercially produced under the tradename "solid state triode."[23] The current flowing out of the SST is a function of both the gate and the drain potentials. Consequently, the SST exhibits the familiar triode-like characteristics as shown in Figure 19. However, the SST operates by potential barrier control rather than relying on the space-charge-limited behavior of the SIT. Published results have demonstrated that these commercial solid state triodes are capable of high power operation into the UHF range and future work is expected to push this limit past one gigahertz.[23]

4.3.3.6 Circuit Integration Issues

The vertical power devices discussed in Sections 4.3.3.2-4.3.3.5 employ the back of the semiconductor wafer for their respective output terminals. It is recognized, of course, that the unique requirements of these types of transistors preclude their monolithic integration, by conventional means, with other circuitry. Fortunately, advanced wafer preparation methods are becoming available which permit circumvention of these difficulties. One such technique involves semiconductor etch and refill as illustrated in Figure 20.[24,25] This method begins by photolithographically defining selected areas on a <100>-oriented, silicon substrate. The regions so defined will, ultimately, house the conventional circuitry ancillary to the vertical power device. In the meantime, material in these regions is etched away using a caustic etch. Subsequently, three layers of epitaxy, alternating in conductivity type, are grown in a single operation. Finally, the composite assembly is mechanically ground back to expose the desired wafer configuration. In the example shown in Figure 20, it is apparent that a vertical transistor can now be fabricated in the center region of the wafer. Flanking this area are a pair of epitaxial islands which are junction-isolated from the central, power device.

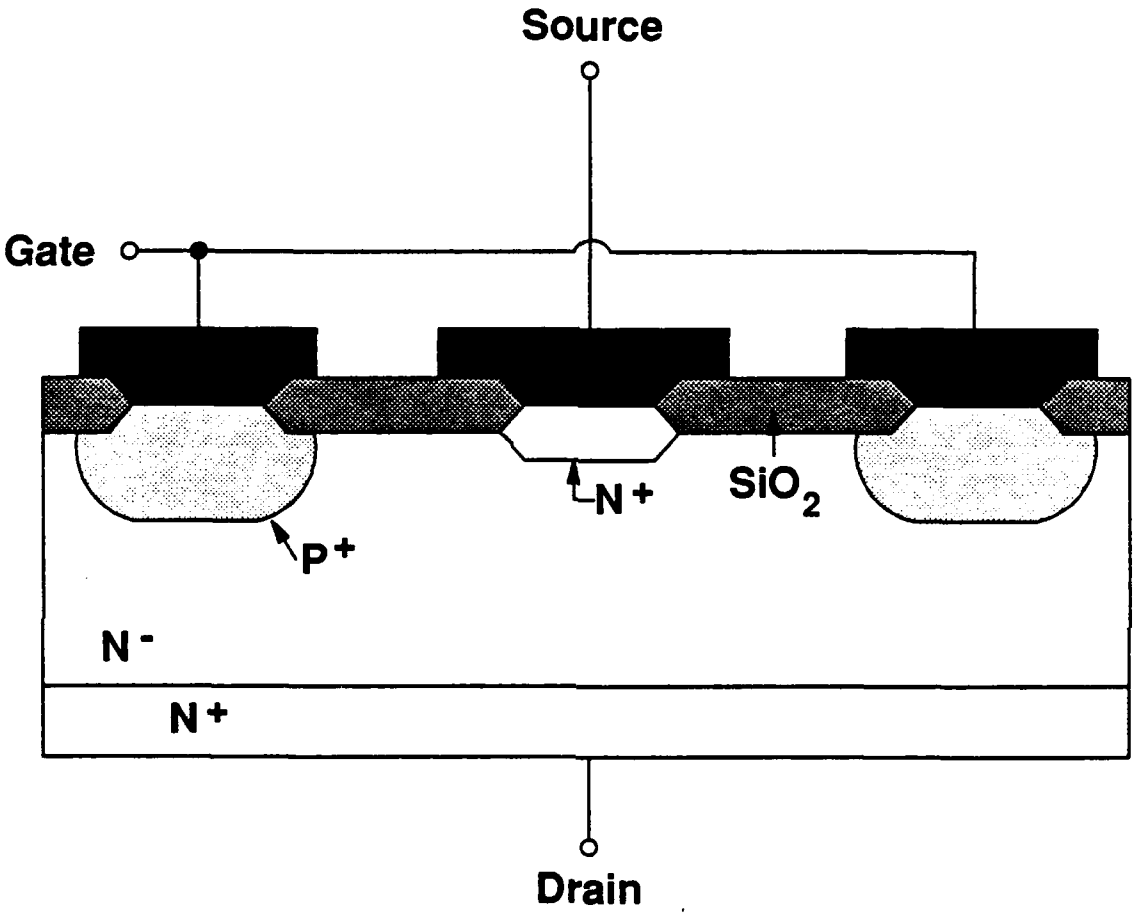

Figure 18. Simplified Cross Section Of A Solid State Triode. (Courtesy Of Adrian Cogan, MicroWave Technology).

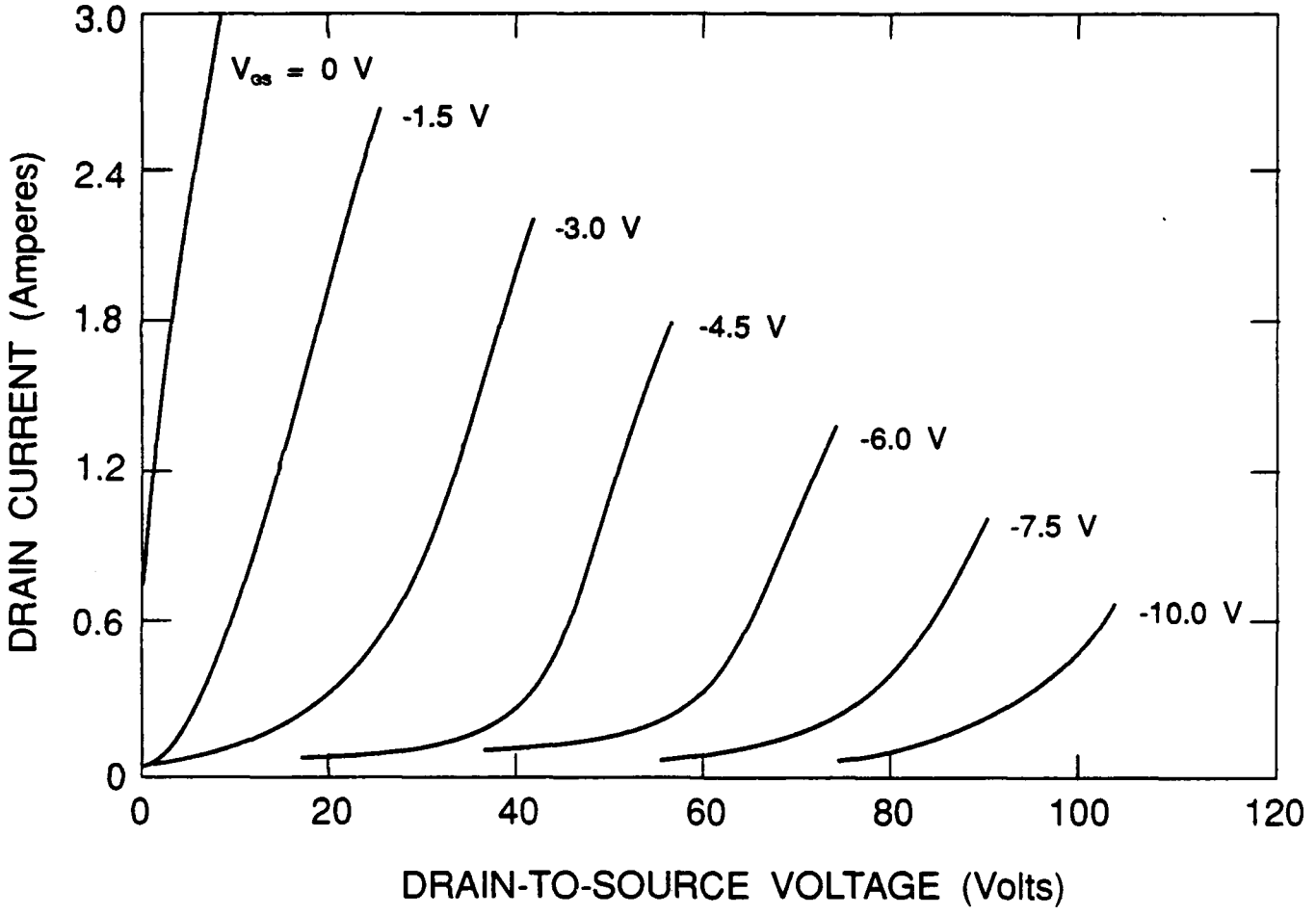

Figure 19. Current Versus Voltage Characteristics For A Solid State Triode. (Courtesy Of Adrian Cogan, MicroWave Technology).

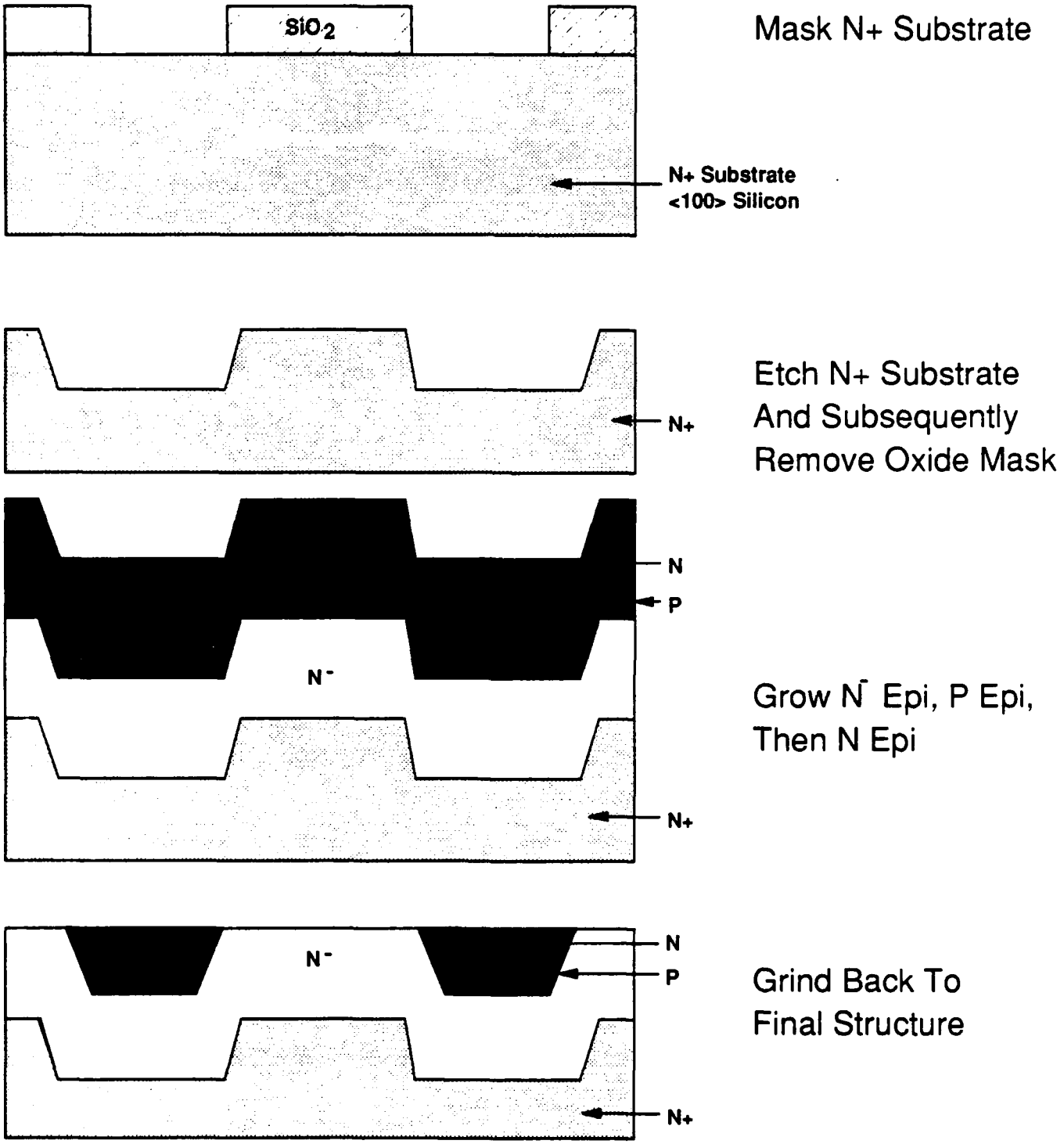

Figure 20. Simplified Schematic Of The Semiconductor Etch And Refill Technique.

4.4 Optimizing the Level of Integration

4.4.1 Comparison of Hybrid and Monolithic Technologies

In hybrid circuitry, the isolation of components is done by physical separation and the subsequent connection of elements is accomplished by extensive use of wire bonds. Because components can be screened prior to assembly, hybrids tend to feature very precise resistors, capacitors and other elements. Consequently, the resulting hybrid module often displays exemplary electrical performance.

Unfortunately, the low level of integration, with its concomitant escalation of assembly cost, tends to make hybrid modules expensive to procure in large quantities.[26] Moreover, the critical steps must be repeated each time an additional module is fabricated. Making, for example, 100 hybrids may consume nearly 100 times the money required to construct a single hybrid. In contrast, monolithic technologies have high levels of integration and, thus, enjoy low assembly cost. Perhaps, the most well-understood monolithic technology is that being employed to build silicon integrated circuits. Georgia Tech believes that several lessons learned over the years by the silicon industry may have direct bearing on the fabrication of UHF radar modules.

4.4.2 Some Lessons From Silicon

Silicon integrated circuits have a number of important characteristics as enumerated in Table 19. Clearly, small size and a reliability enhancement incurred via the elimination of wire bonds are consequences of converting from a hybrid technology to an integrated approach. Furthermore, because components can be fabricated very close together on the same chip, devices tend to match well on integrated circuits.

Integrated circuit designers like to use high levels of integration and, in fact, the number of components in the most advanced integrated circuits has doubled every year since 1959.[27] This observation was made by Gordon Moore in 1964 and, as seen in Figure 21, has remained true for the ensuing two decades. This increased level of integration provides the customer with more

Small Size

High Reliability

Matched Devices

High Level Of Integration

Low Cost

Improved Performance

Obey A Steep Learning Curve

Table 19. Some Characteristics Of Silicon Integrated Circuits.

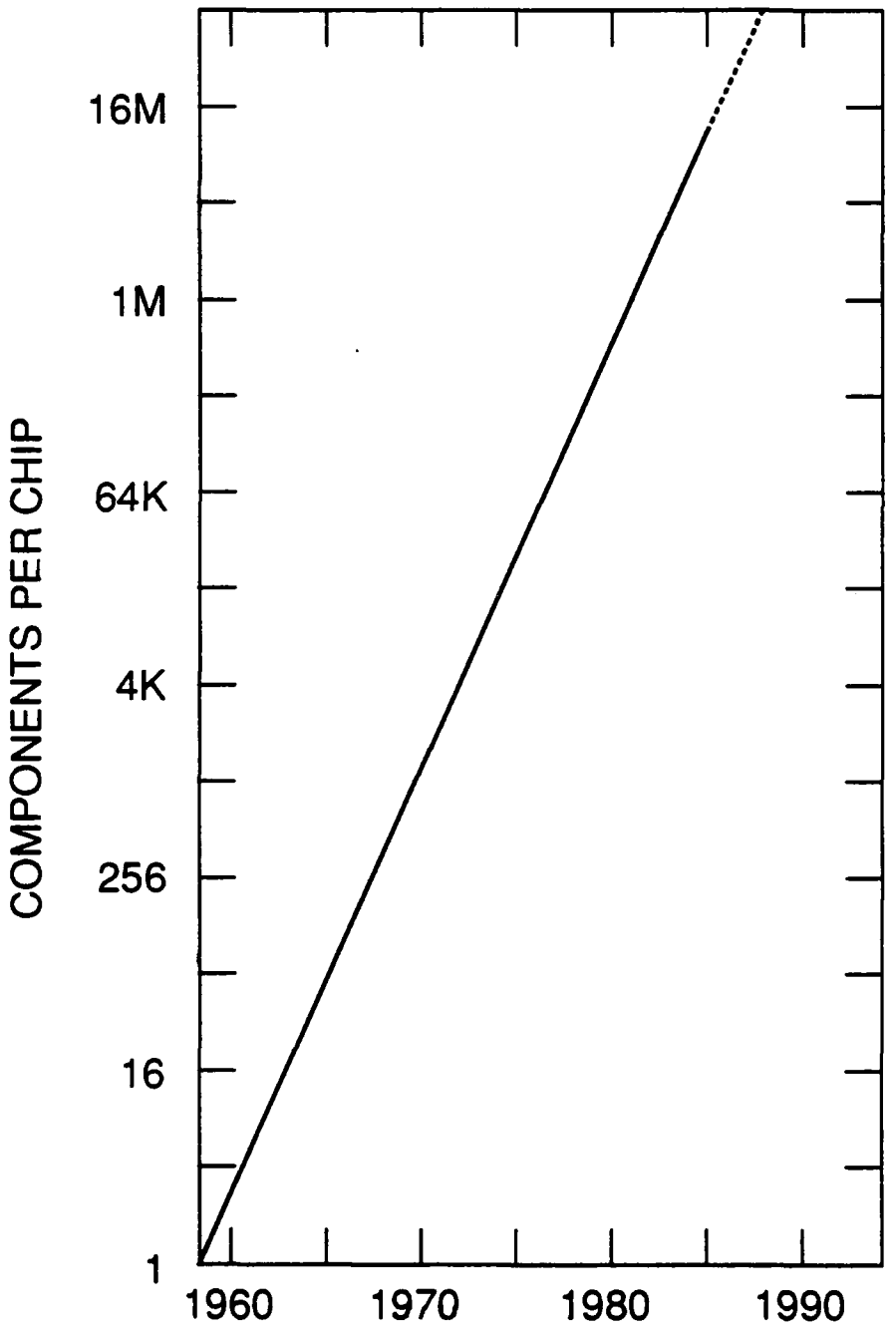

Figure 21. An Illustration Of Moore's Law.

functionality. Furthermore, any initial price premium is cheerfully absorbed because high levels of integration can reduce the other overhead costs for a deployment. In essence, a sophisticated integrated circuit enables the customer to obtain a comprehensive solution to his system problem on a single chip.

The low cost of integrated circuitry is engendered by the inherent advantages of batch processing of the semiconductor wafers. With batch processing, all of the chips get exposed to, for example, the isolation diffusion at the same time. Consequently, the cost of making one or many identical components is essentially the same. These "free" extra components can be used to create more circuitry and, thus, improve system performance or add redundancy to the chip. Furthermore, batch processing suggests that success on even a single wafer can yield many good circuits.

Additionally, silicon integrated circuits obey a steep learning curve. In practice, a learning curve quantifies the notion that manufacturers get better at fabricating a given item as they gain experience in its production. Several example learning curves are plotted in Figure 22 and illustrate that the cost, in constant dollars, incurred in the manufacture of a given product falls by a fixed amount each time that the cumulative output of that product doubles. For instance, the 70% learning curve reveals that each time the cumulative production of an item doubles, the cost becomes 0.70 times what it was before that doubling.

Table 20 summarizes the historic learning curve coefficients for selected silicon integrated circuit families. It is apparent that an aggregate learning curve for this industry is of the order of 70%.[27] The steepness of this curve is important because it confirms that integrated circuit producers can accrue cost-savings experience fast enough to actually reduce the retail price of their products with time. Trusting in this phenomenon, new chips can be brought to market when their yields are only a few percent. The yields improve rapidly as the volume escalates and the costs fall correspondingly. Some additional consequences of a steep learning curve are outlined in Table 21.

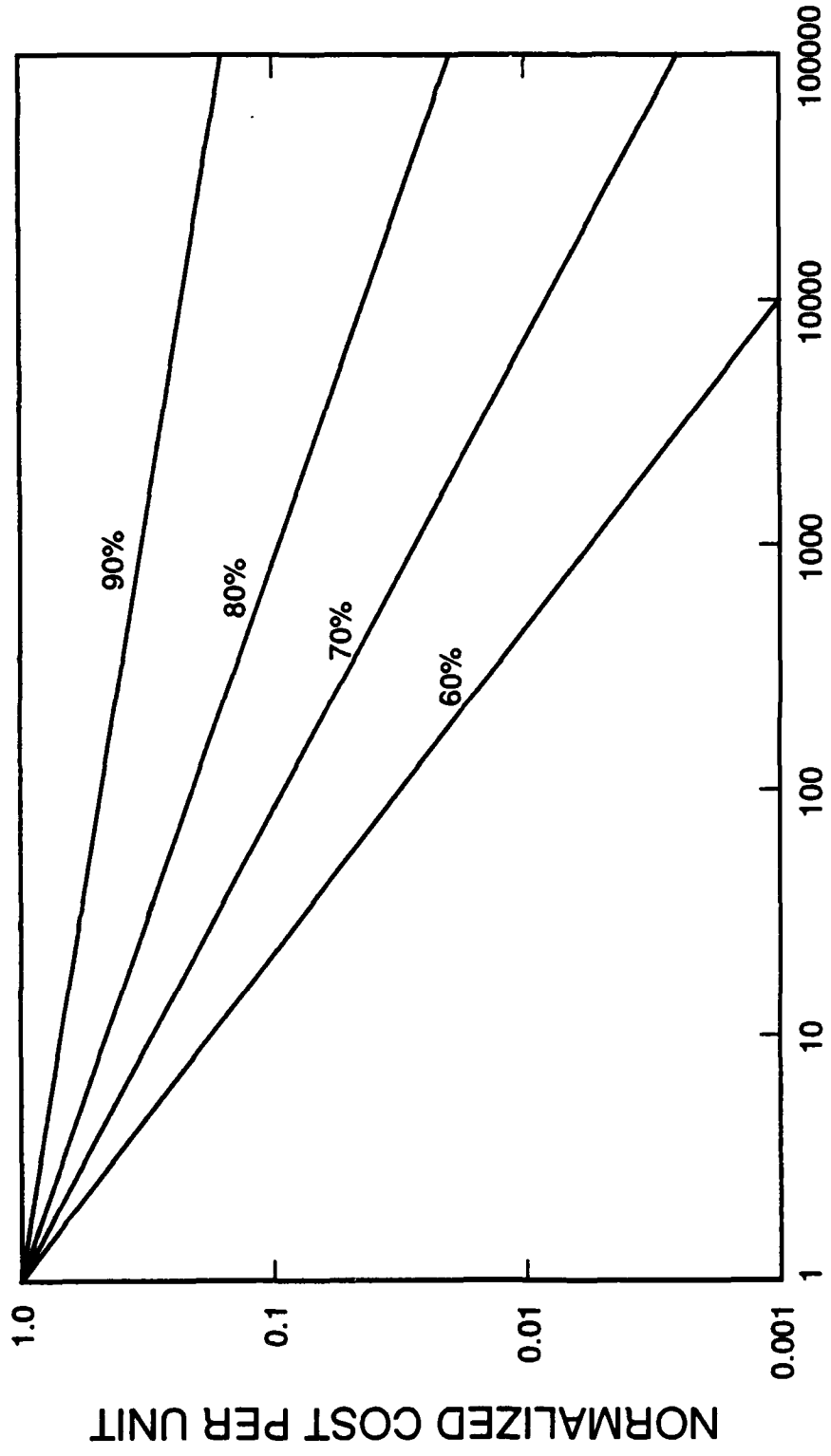

Figure 22. Examples Of Learning Curves.

Bipolar ICs	72%
MOS LSI Chips	80%
MOS DRAMs	68%
IC Gates	60%
Average	70%

Table 20. Historic Learning Curve Coefficients For Selected Integrated Circuit Families.

Technology and marketing targets move rapidly

Getting there first has significant cost and profit advantages

This yields large payoffs to successful mobilizers and large penalties for those who aren't

The "old guard" in the electronics business haven't been able to dominate the silicon integrated circuits arena

Table 21. Some Consequences Of A Steep Learning Curve.

A final lesson from the silicon integrated circuits industry involves the very limited proliferation of different wafer processes. As an example, most silicon bipolar integrated circuit wafer processes are designed to make vertical NPN transistors. Ideally, the circuit designer is instructed to make use of the fundamental NPN transistor whenever possible. For instance, an NPN can be used as a current source, a diode or a resistance load. When unusual diodes, PNP transistors or resistors are required, the wafer process is not changed. Instead, the masks are modified to allow the same process to yield these variations on the basic NPN structure. Many products including amplifiers, voltage regulators, power control circuits, telephone switching gear and data conversion parts all use the same wafer process. Only the masks are changed. The underlying process is soon perfected and turns out the same characteristic parameters day in and day out. Yield is good and the performance of the resulting chips is both predictable and reproducible. Even the high volume, silicon bipolar participants follow the adage, "No product is worth its own wafer process."

4.4.3 Silicon-Based UHF Integrated Circuits

4.4.3.1 Introduction

Georgia Tech believes that integrated circuits will find increasing use in all but the highest power UHF radar modules. The insertion of such chips is expected to significantly decrease the packaging, assembly and testing cost overhead handicapping current modules.[9,28-31] It is further anticipated that several standard wafer processing flows can ultimately serve as the workhorses for this marketplace. Hopefully, the escalating demand for UHF integrated circuits by the commercial, industrial and consumer sectors will help to accelerate the development of fabrication facilities and expertise.[30]

As pointed out by R.H. Chilton and discussed in Section 4.3.3.1, it appears unlikely that gallium arsenide monolithic microwave integrated circuits (MMICs) will be either appropriate or cost-effective at UHF.[3] It seems safe to suggest, however, that

silicon-based integrated circuits deserve a serious look for UHF module deployments.[32]

4.4.3.2 Dielectrically Isolated Integrated Circuits

High frequency integrated circuits are beginning to appear on dielectrically isolated silicon.[33,34] Fundamental to this process is the ability to prepare the substrate material itself using the process outlined in Figure 23. These important operations rely on the use of a caustic etch to create V-grooves in <100>-oriented silicon. Subsequently, the material is oxidized to form the dielectric liner for the device tubs and backfilled with a thick layer of polycrystalline silicon. Then, the majority of the original, single-crystal material is lapped away to form the indicated structure. At this point, one vendor caps the material with an epitaxial layer for use in their dielectrically isolated, monolithic microwave integrated circuit (DIMMIC*) process.[33,34] In any event, standard semiconductor processing is finally employed to fabricate the desired circuit elements in adjacent tubs. Figure 24 shows a simplified cross section through an NPN transistor formed on the DIMMIC process.

It is apparent that dielectric material features low parasitics and excellent isolation between tubs and, thus, provides the potential for high speed, low crosstalk and high voltage operation. In addition, the associated confinement of any induced substrate currents permits the corresponding circuit to enjoy good immunity from transient radiation upset. However, the silicon dioxide required for the tub liners has only a moderate thermal conductivity. Consequently, circuits formed on dielectrically isolated material will, probably, be limited to several tens of watts of power dissipation.

Available data show successful operation beyond 1 GHz and it is hoped that dielectrically isolated integrated circuits will find significant application in the high speed, low density, medium power marketplace.[33]

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* DIMMIC is a trademark of Motorola, Inc.

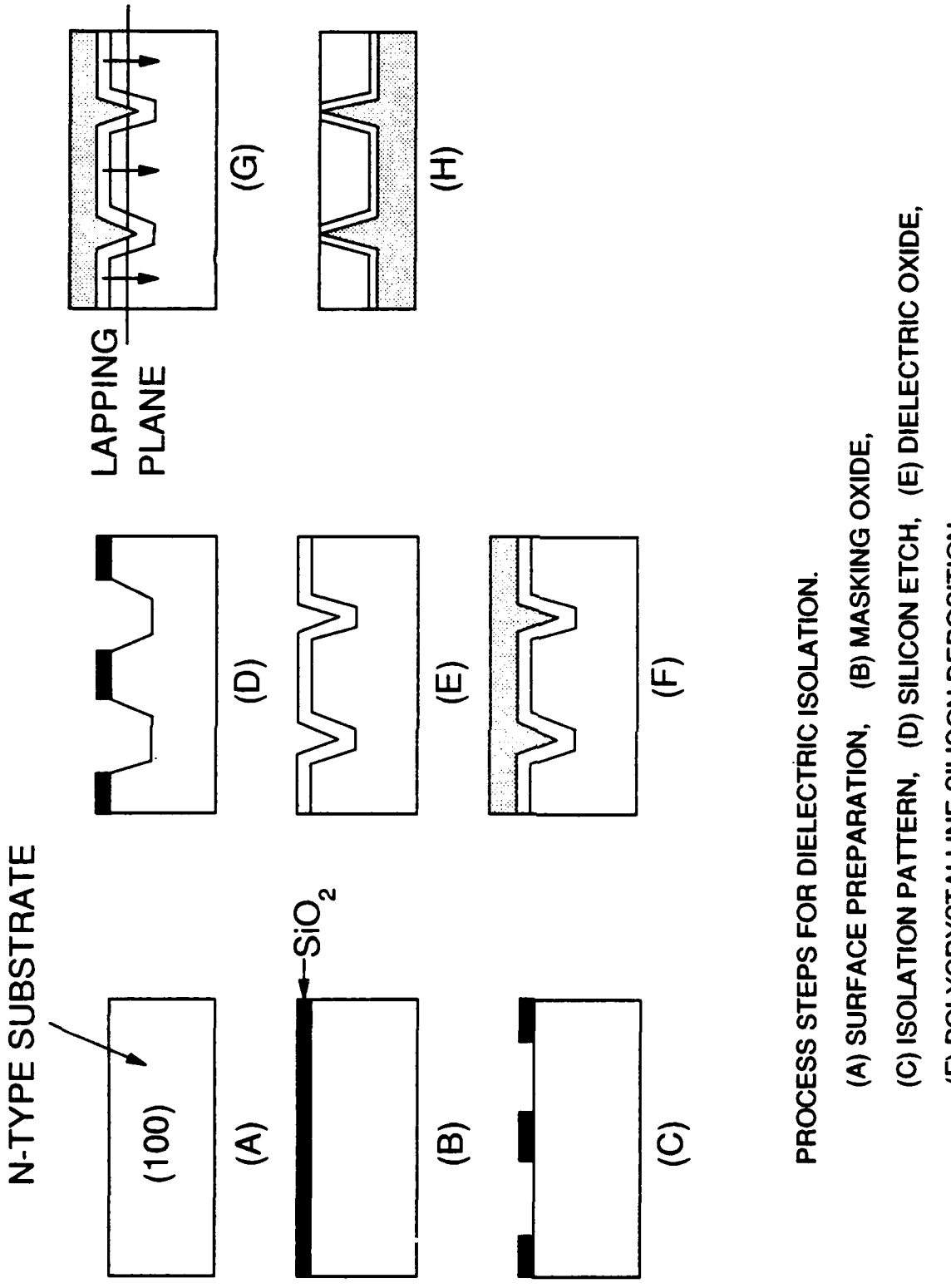

Figure 23. The Basic Processing Steps For Preparing Dielectrically Isolated Material.

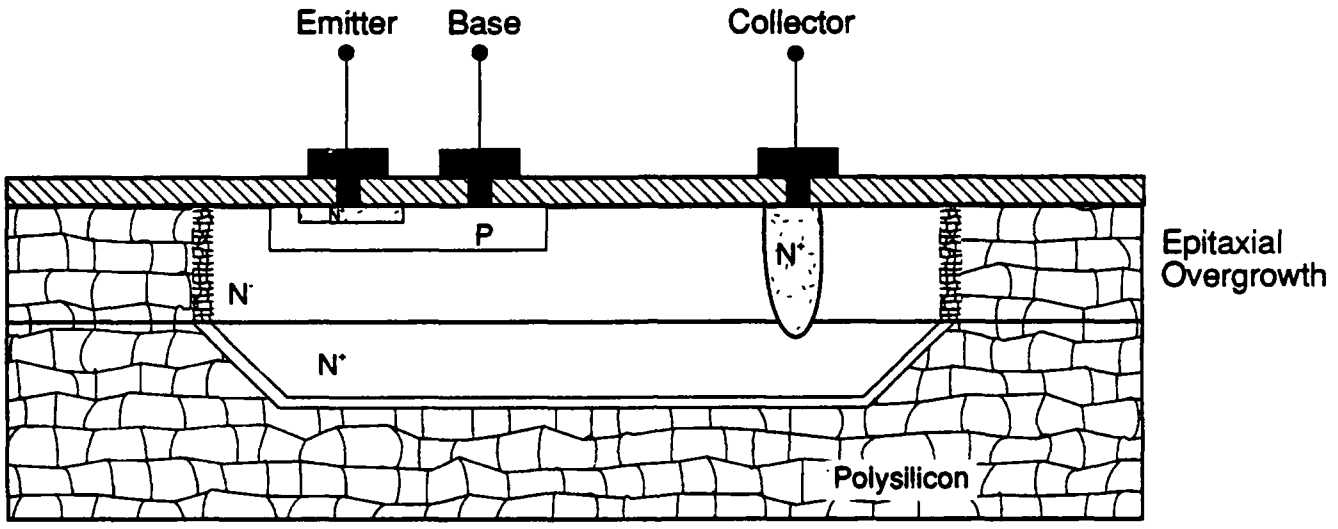

Figure 24. Simplified Cross Section Through An NPN Bipolar Transistor Formed On The DIMMIC Process. (Courtesy of Pete Bachert, Motorola).

4.4.3.3 Oxide Sidewall Isolated Integrated Circuits

Another wafer processing technology which seems deserving of evaluation for UHF is that which relies on oxide regions to provide only lateral isolation of inegrated circuit elements. Originally developed for digital applications, the various oxide sidewall isolation processes yield transistors which can operate well into the microwave regime. Perhaps, the earliest technology of consequence in this arena was the ISOPLANAR process developed by Fairchild.† Other firms followed suit with their own variations and names like MOSAIC** are, now, commonly heard. One vendor has developed a related process called ISOSAT specifically for MMICs.††[35,36]

Figure 25 presents a simplified cross section through a bipolar transistor formed on the ISOSAT process and illustrates the salient features of the oxide sidewall approach. Notice, in particular, the use of recessed, planar field oxide and trenches for device isolation. In addition, the emitter and base are self-aligned resulting in small devices and reduced parasitics. Consequently, the transistors enjoy extremely high cutoff frequencies for a silicon-based technology. With continued progress, it is believed that some version of the oxide sidewall isolated technologies will be useful for high speed, high density, low power deployments.

4.4.3.4 Circulators and Integration

When considering the exclusive usage of integrated circuits for transmit/receive modules, the circulator function becomes particularly problematic. Attempts to silk screen ferrite material onto appropriate substrates has met with limited success, but the required processes are not typical of those used in conventional integrated circuit fabrication. Consequently, some workers have

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† ISOPLANAR is a trademark of Fairchild, Inc.

** MOSAIC is a trademark of Motorola, Inc.

†† ISOSAT is a trademark of Avantek, Inc.

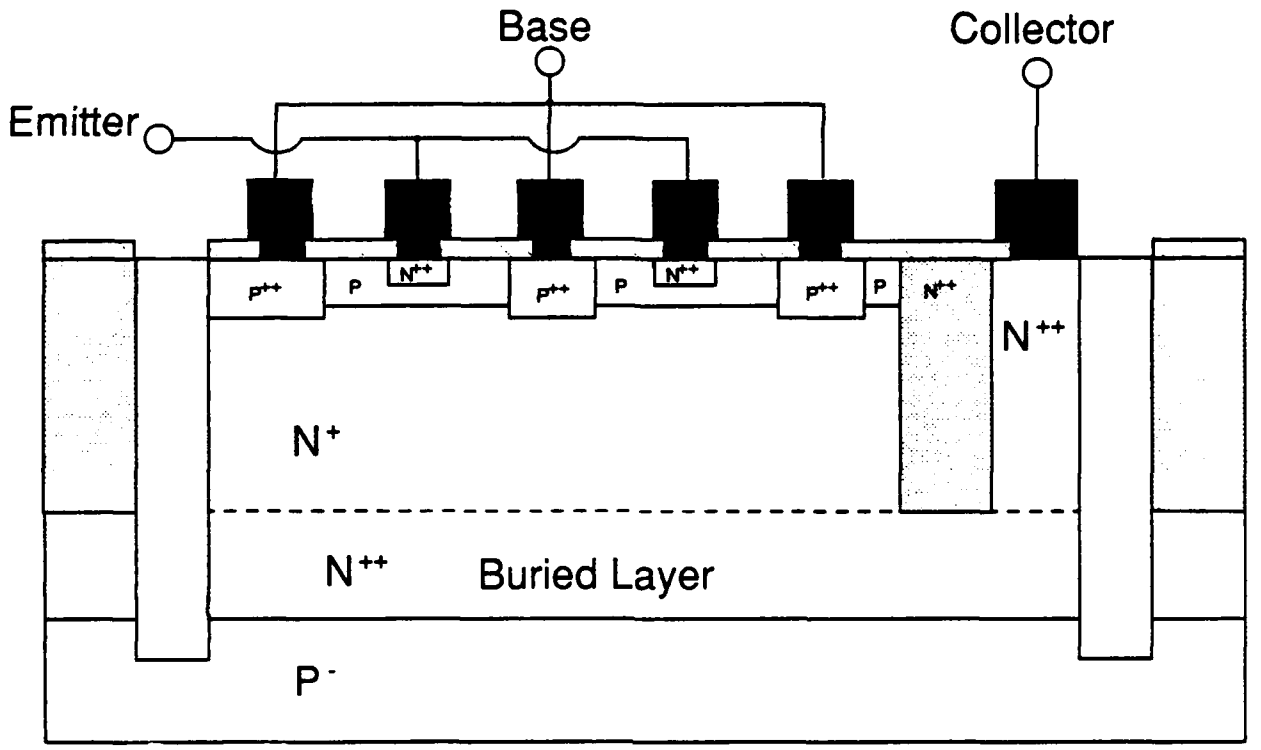

Figure 25. Simplified Cross Section Through An NPN Bipolar Transistor Formed On the ISOSAT Process. (Courtesy of Craig Snapp, Avantek).

advocated making circulators from the active transistors themselves. Unfortunately, early realizations of such hardware suffered from the problems enumerated in Table 22.

Recent research on active circulators, however, has overcome two of these common difficulties.[37] The electrical schematic sketched in Figure 26 has recently been employed to fabricate an active circulator on a 63x63 mil chip. The source nodes of gallium arsenide MESFETs Q_1, Q_2 and Q_3 are returned to ground through the common, series-feedback impedance supplied by Q_0. The resulting circuit operates from 1-5 GHz provides a minimum of 15 dB of isolation and enjoys an insertion loss of less than 5 dB.[37] In fact, the 5:1 bandwidth is exceptional for even ferrite-based devices and the active circulator is highly compatible with conventional wafer processing.

4.5 Trimming

4.5.1 Introduction

High frequency integrated circuits need to be adjustable in order to ensure that they are operating according to the required specifications. The desired adjustments are often called "tweaks" or "trims" and can be used to compensate for electrical skew caused by variations in the manufacturing process.

In the hybrid arena, such tweaking is frequently done by substitution of components, mechanical manipulation of trimming tabs or adjustment of external power supplies. Unfortunately, these elementary tweaking techniques cannot be amenably applied to integrated circuits. Thus, as a natural consequence of wafer processing variations, the resulting chips either fail to achieve their parametric goals or, in extreme cases, do not function at all. Therefore, the yield of the product is low and the concomitant cost of the enterprise is unnecessarily escalated. Furthermore, experience has shown that manufacturing variations tend to have an increasingly severe impact on yield as the complexity of the integrated system itself evolves. In the limit, of course, a large scale integrated circuit may, in fact, consistently have a trivial yield.

Limited Bandwidth

Excessive Loss

Poor Noise Figure

Table 22. Common Problems With Non-Conventional Circulators.

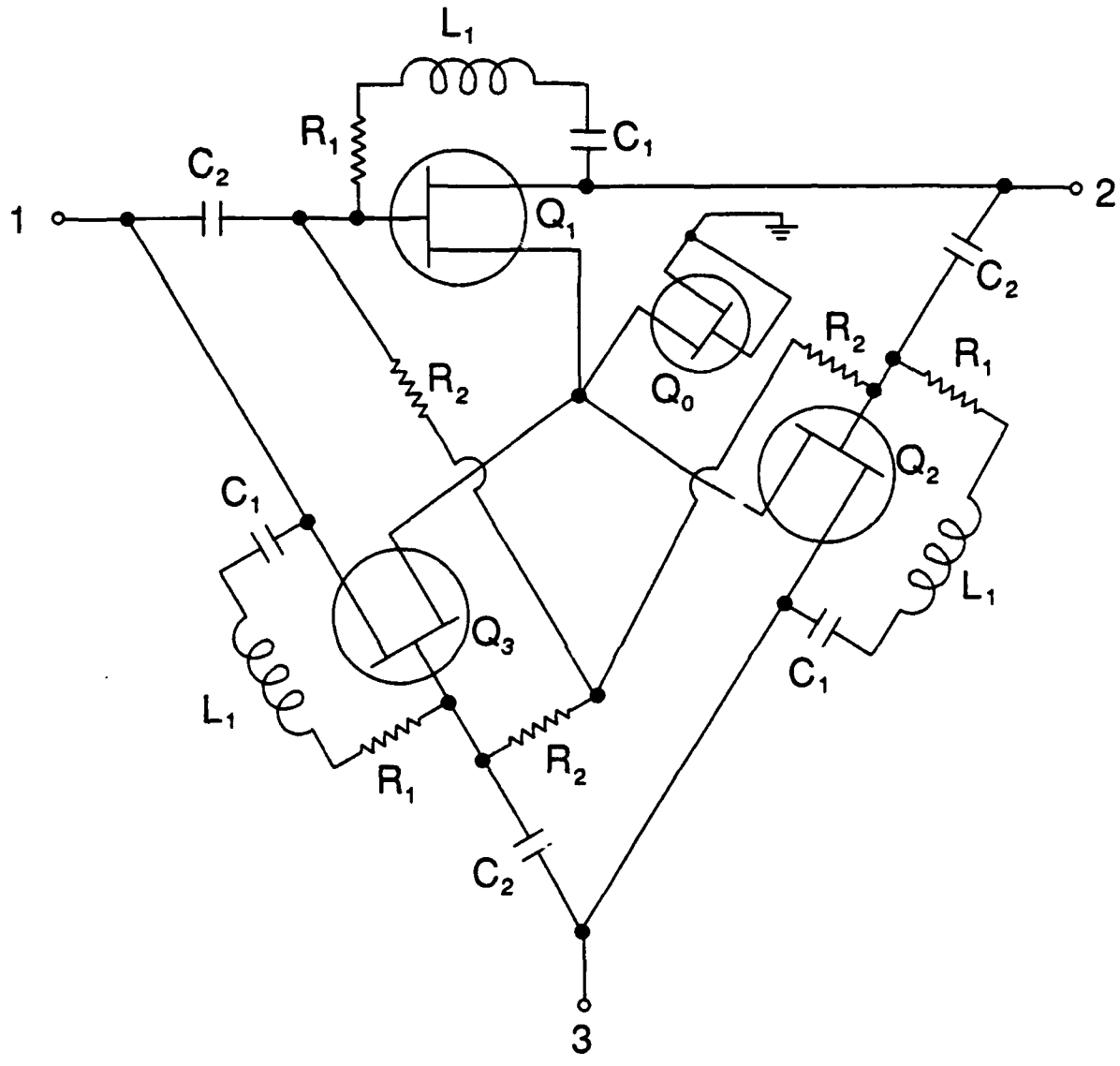

Figure 26. Schematic Diagram Of MESFET-Based Circulator. (After Dougherty, Reference 37).

Some members of the high frequency integrated circuit community have begun to recognize the need to eliminate wafer processing variations in order to force high performance chips to produce a satisfactory yield.[38] Such a capability is particularly important for analog circuits because of their stringent requirements on parametric quantities.

It is valuable to be able to tweak, for instance, the bias point of a gallium arsenide (GaAs) metal-semiconductor field effect transistor (MESFET). Such transistors are easily fabricated with a GaAs wafer process and are commonly used as amplifying elements in MMIC chips. The design of the corresponding MMIC amplifier is often done by means of a scattering-parameter (S-parameter) approach. In any event, the ultimate performance of the circuit is determined by the S-parameters of the transistor element itself. These parameters, in turn, are a function of the bias conditions of the MESFET. Thus, trimming the operating point of the FET changes the tuning of the amplifier as shown in Figure 27.[39] It is apparent that the characteristic gain of this X-band amplifier is degraded significantly if the operating point is not set precisely to its nominal value.

As a second example of the utility of trimming, assume that it is desired to have a resistance of 100 ± 6 percent ohms between two nodes. Furthermore, presume it is known that the typical processing scatter on such resistors is ±10 percent. Clearly, a 10 percent processing variation is not ideal for building circuits that can tolerate only a 6 percent variability. However, if the circuit is capable of being trimmed, a significant improvement in yield can be realized. Table 23 summarizes a number of possible outcomes that can be attained by trimming the circuit in Figure 28. It is apparent from Table 23 that a considerable yield enhancement is enjoyed by the trimmed dice by using even the simple trimming arrangement outlined in Figure 28. Clearly, a more comprehensive trimming network having both series and parallel options would be even more successful in eliminating the effect of wafer processing variations.

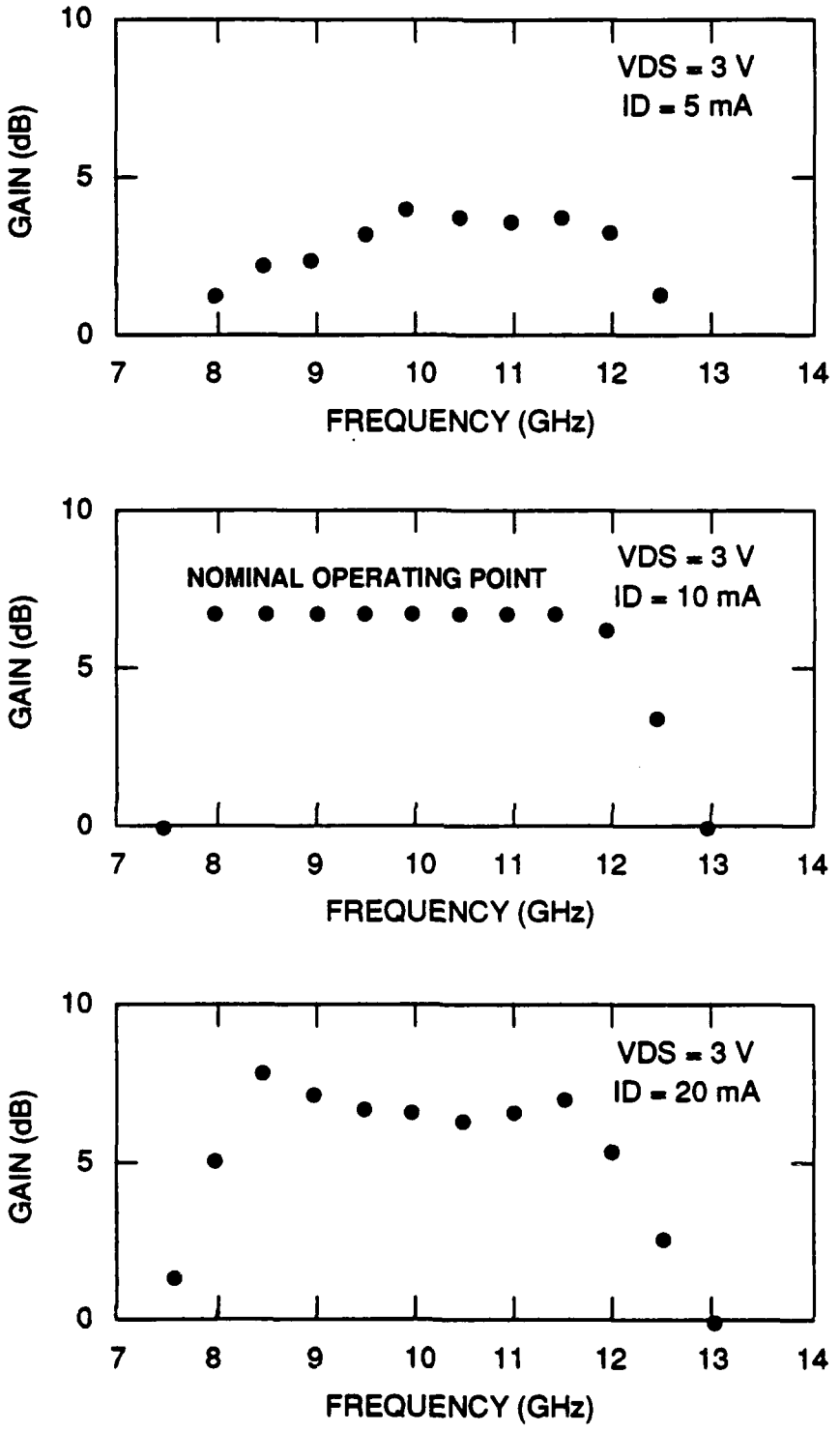

Figure 27. The Performance Of An X-Band Amplifier As A Function Of Its Operating Point.

Pre-Trim Resistor Value	R10, 20 Before Trim	Yield Before Trim	Close Sa	Close Sb	R10, 20 After Trim	Yield After Trim	Remarks
Nominal	105.00	Yes	No	No	105.00	Yes	No trimming required when processing is on target.
Nominal	105.00	Yes	Yes	No	100.00	Yes	Tweaked to ideal value even though processing is on target.
+10%	115.50	No	No	Yes	104.50	Yes	
-10%	94.50	Yes	No	No	94.50	Yes	
+5%	110.25	No	Yes	No	105.00	Yes	
+5%	110.25	No	No	Yes	99.75	Yes	Even better than previous option.
-5%	99.75	Yes	No	No	99.75	Yes	
+15%	120.75	No	Yes	Yes	103.50	Yes	Successful trim even though processing is out of spec.
-15%	89.25	No	No	No	89.25	No	Processing out of spec. Beyond trim range.

Table 23. Some Possible Outcomes Of Trimming On The Circuit Illustrated In Figure 28.

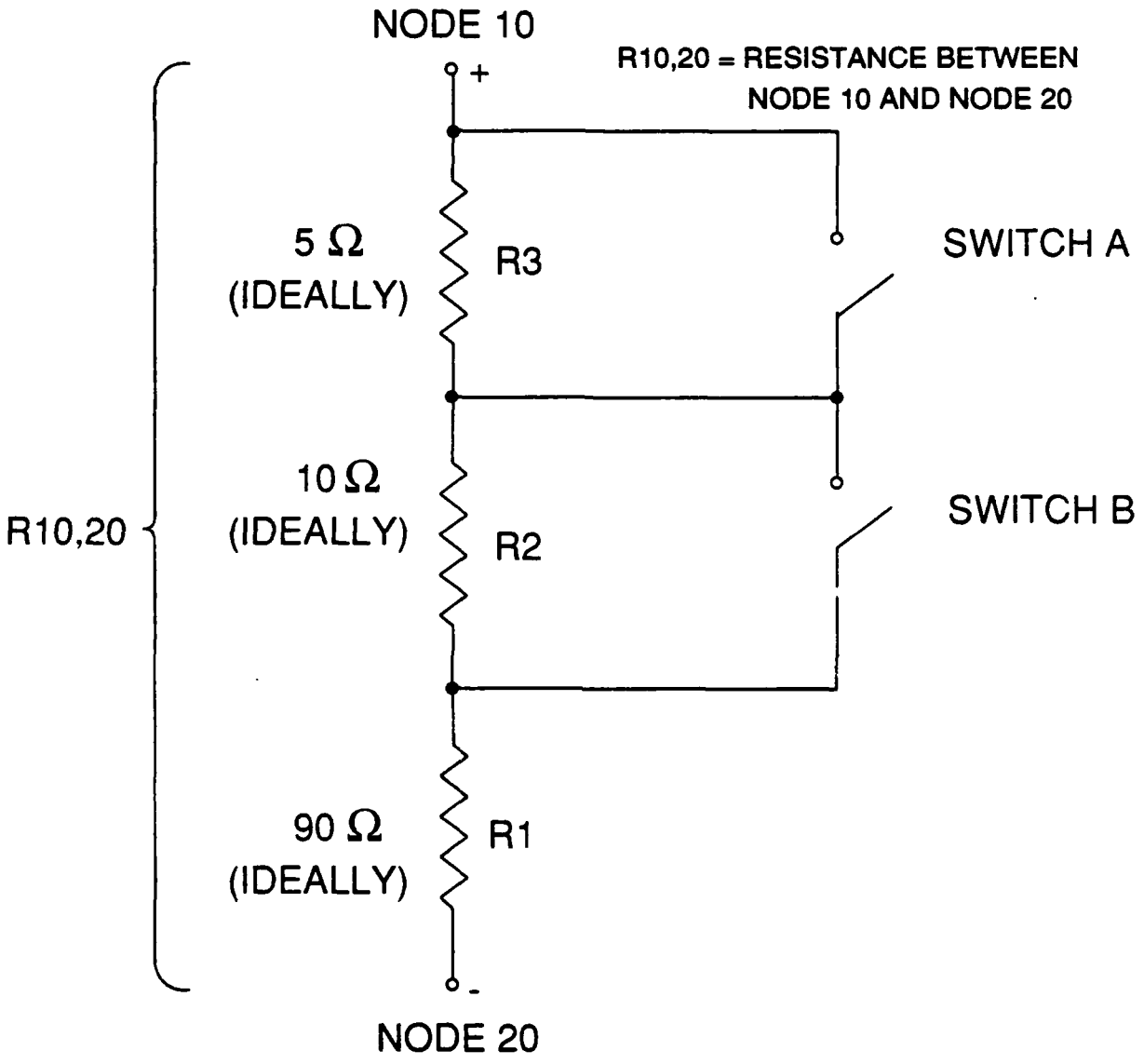

Figure 28. One Way Of Trimming A Resistor String.

In addition to the methods outlined above, a number of other trimming techniques are currently being employed by the semiconductor industry. The majority of these methods involve patching elements in or out of the active circuitry, as required, by creating either shorted regions or open circuits.[40-44] Both lasers and electrically fusible links are extensively used to achieve the requisite shorts or opens. Alternatively, aluminum from a plurality of contacts can be spiked into the body of an integrated circuit resistor.[45] This has the effect of trimming the electrical length of the resistor to a value smaller than that corresponding to its apparent physical length.

Previous research has demonstrated that it is possible to automate the testing and trimming of electronic circuits. An automated methodology particularly germane to high frequency componentry is elucidated in Figure 29. This technique involves the use of a computer-driven manipulator for perturbing the performance of the untrimmed circuit. After performing a sequence of perturbations, the test algorithm forms a response matrix for the circuit and, thus, is able to calculate the required adjustment. Finally, this adjustment, or trim, is executed by, for example, a laser cutting away on a microstrip tab. Because of the physical dimensions of the probes employed for the perturbation step, the approach outlined in Figure 29 is best applied to hybrid circuitry. However, Georgia Tech believes that advanced implementations using charged-particle beams or photons for perturbation may allow the extension of such a technique to integrated circuit geometries.

Regardless of the details, conventional trimming techniques such as those discussed above share the features summarized in Table 24.

4.5.2 The TECH-TRIM Technology

Georgia Tech has developed and patented a novel trimming technique coined TECH-TRIM which can easily be applied to integrated circuits.[46] The new method does not necessarily inflate the component count nor does it significantly complicate the chip

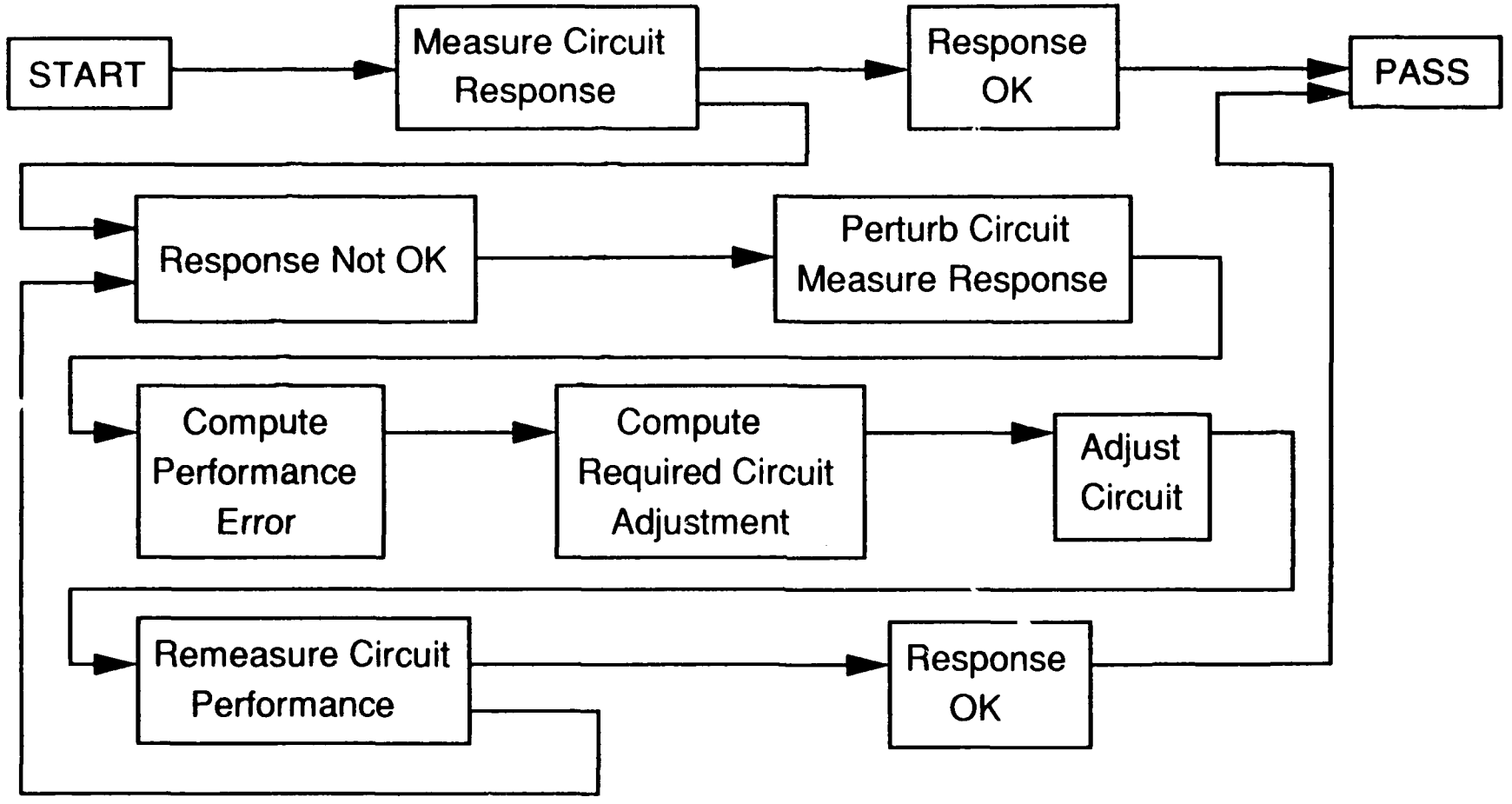

Figure 29. Flow Chart For One Method For Automatic Trimming Of A Circuit. (Courtesy Of Bob Gardenghi, Westinghouse).

Trimming can be used to make non-functional parts yield and, in addition, can make functional parts parametrically superior.

Trimming can give the manufacturer the capability to adjust out processing variations and assembly shifts. In the future, it may afford the customer the possibility of field adjustment and repair.

To capitalize on trimming, it is necessary to design in the capability to trim the circuitry of interest.

More demanding chips and/or highly variable manufacturing processes engender more complex trimming circuitry.

Conventional trimming inflates the component count and, hence, the chip size in an attempt to tweak out the inevitable manufacturing variations.

Table 24. Some Characteristics Of Conventional Trimming Techniques.

design. TECH-TRIM was invented on internal funds prior to the present contract, but the technology may be germane to future UHF modules.

The new methodology is based upon the introduction of systematic and repeatable changes in device parameters by energetic pulses applied between appropriate terminals. Consider, for example, the bipolar current source illustrated in Figure 30. Such a source is often called a "current mirror" and comprises a technique for deriving a family of currents from a single, reference current. Notice that transistor Q_0 is wired to behave like a diode and, thus, the current in its respective branch is given by Equation 1.

$$I_0 = I_{s0} [\exp (qV_0/kT) - 1] \simeq I_{s0} [\exp (qV_0/kT)] \qquad (1)$$

where: I_{s0} = reverse leakage current of the emitter-base junction for transistor Q_0

q = charge on an electron

V_0 = diode forward voltage

k = Boltzmann's constant

T = absolute temperature

Further note that transistors Q_1 and Q_2 are connected such that $V_2 = V_1 = V_0$. Hence, I_1 and I_2 will equal I_0 if all three transistors have the same leakage current. They will, in general, have the same leakage if their respective emitter-base junctions are identical. If, however, Q_2 has, for instance, twice the emitter area of Q_0 and Q_1, then I_2 will be double I_0 and I_1. In use, I_0 is the source reference current while I_1 and I_2 feed bias lines for active devices in the adjacent circuitry.

Of course, as a consequence of manufacturing variations, the current in the bias legs will rarely be perfectly ratioed. This is particularly unfortunate because the performance of a chip can be a sensitive function of the various internal bias points. Clearly, what is needed is a way to trim the bias lines in order to tweak the operating points of the corresponding transistors.

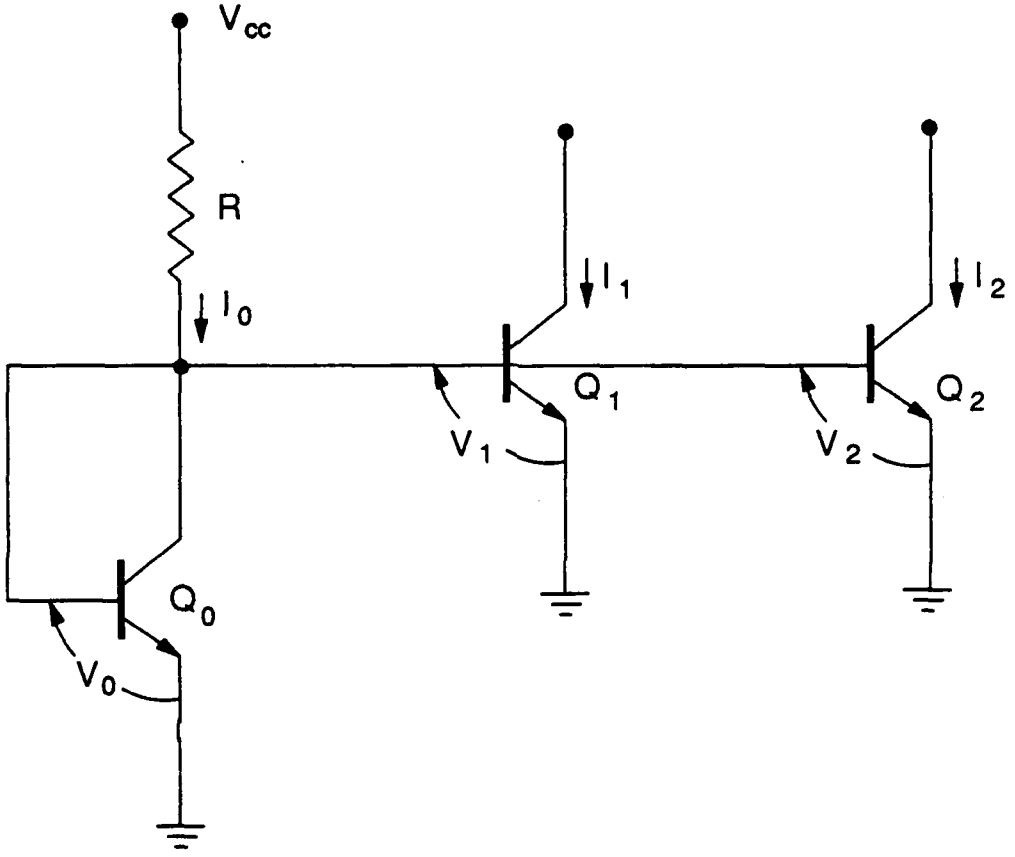

Figure 30. A Bipolar Current Mirror.

TECH-TRIM has been used to successfully trim the current mirror illustrated in Figure 30. It is believed that the intentional reverse-bias pulsing of the emitter-base diode drives metallics through the highly dislocated, phosphorus-doped emitter region toward the junction. These metallics, presumably, increase the recombination velocity at this critical junction and, hence, modify the beta of the corresponding transistor. In any event, the current ratios in the bias legs have been trimmed by as much as a factor of two. Furthermore, annealing tests have demonstrated little tendency for similarly-adjusted silicon integrated circuits to drift away from their trimmed value.

It should be remarked that TECH-TRIM may be easily extended to trimming of the input offset voltage on differential amplifiers or to adjust the performance of similar, balanced circuitry. The capability to achieve such goals is apparent from an examination of Figure 31 and Figure 32.

Figure 31 presents a simplified schematic of a typical bipolar operational amplifier such as the LM 307. Note that there is an inverting input, In^-, in addition to the In^+ noninverting input. Ultimately, a gained-up difference between the signals at these two inputs appears at the output. Thus, exercising the inputs with identical signals will, ideally, result in no signal at the output. In practical cases, however, some signal usually appears at the output even when the inputs are driven together. In this event, the differential signal which must be applied to the inputs in order to force the output error to zero is called the "input offset voltage" or Vio.

A simple way to estimate the value of Vio for a real operational amplifier is illustrated in Figure 32. Note that the inputs are both tied to the same potential. Furthermore, the closed-loop gain of the circuit is set up to be equal to 100. Thus, the value of the output signal is approximately 100 times Vio.

Now, referring back to Figure 31, it is apparent that Vio can be either a positive or a negative value. A positive value might occur because transistor Q_1 has a higher gain than transistor Q_2.

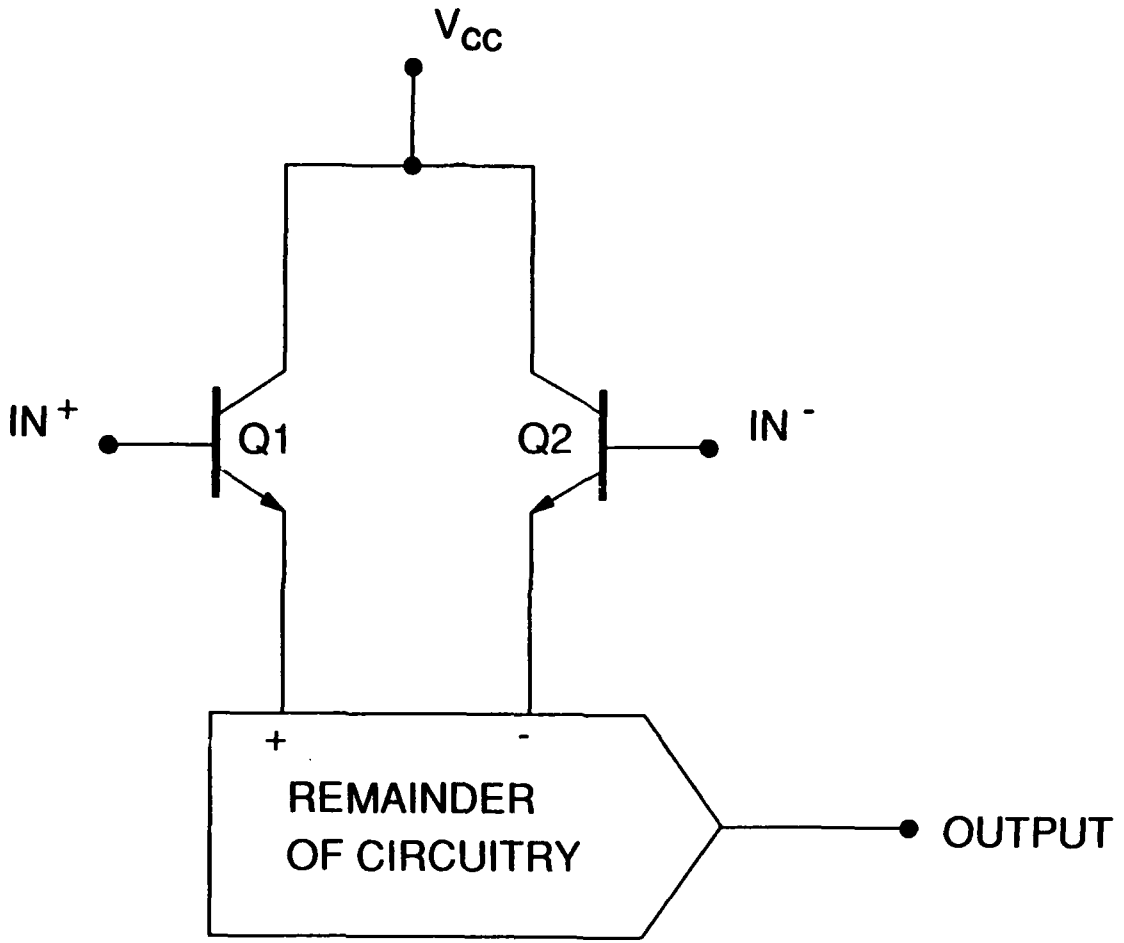

Figure 31. Simplified Schematic Of A Typical, Bipolar Operational Amplifier.

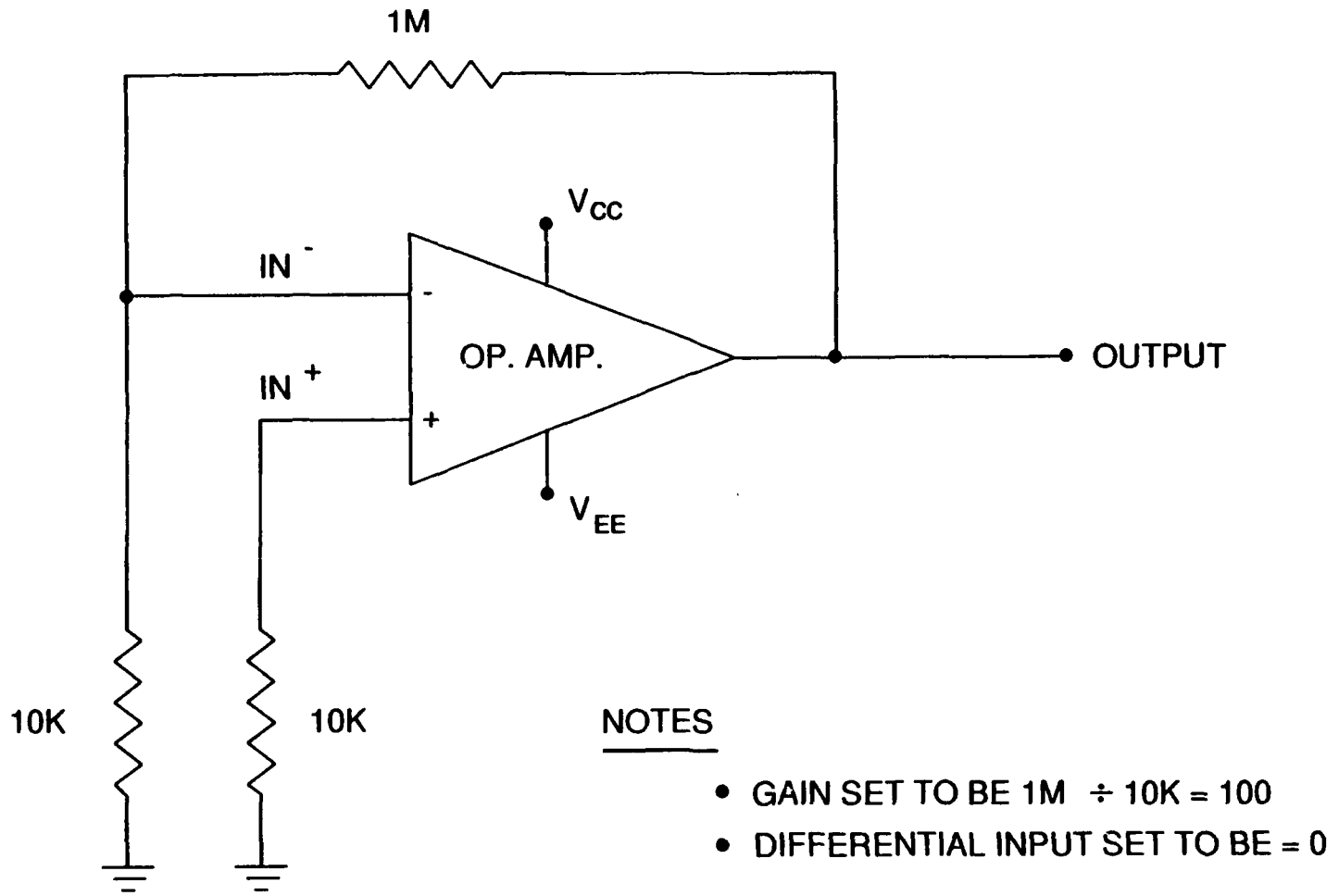

Figure 32. Simplified Circuit For Estimating V_{io} Of An Operational Amplifier.

Such a situation may be readily fixed by using TECH-TRIM to slightly degrade the gain of Q_1. In particular, TECH-TRIM is used to energetically pulse the collector-base junction of Q_1. Further note that, in this example, such trimming can be accomplished from outside the package by using the In^+ and Vcc terminals. Similarly, if Vio is negative, TECH-TRIM can tweak the gain of Q_2 in order to reduce the magnitude of Vio.

TECH-TRIM has been used to successfully trim the Vio of operational amplifiers such as those illustrated in Figures 31 and 32. Such trims have consistently reduced the Vio by up to 4 orders of magnitude and, thus, provide a tool for converting reject parts into salable, premium products.

4.5.3 Description of Demonstration Equipment and Procedures

A number of experiments have been performed which illustrate the application of TECH-TRIM to solid state devices. These demonstration vehicles include, but are not limited to, NPN and PNP bipolar transistors, N-channel JFETs, bipolar current mirrors and operational amplifiers.

As discussed in Section 4.5.2, preferred manifestations of TECH-TRIM involve the application of an energetic pulse or pulses between the terminals of an active component. The desired energy is in excess of that experienced by the device under normal operation and has the effect of modifying the parameters of the device without destroying its utility for the intended application. If, for example, it is desired to TECH-TRIM a bipolar transistor, one may apply either reverse-bias or forward-bias excitation across the terminals of interest. For bipolars, these terminal combinations include the emitter-base, the collector-base and the collector-emitter pairs. Furthermore, the trimming excitation may exercise emitter pairs such as those found in transistor-transistor logic (TTL) circuits. Similarly, it is possible to trim between collectors in the case of, say, integrated injection logic (I^2L) or split collector PNPs.

4.5.4 A Selection of Laboratory Results Achieved With TECH-TRIM

Table 25 illustrates the results of trimming bipolar transistors by exercising various pairs of pins. Note that it is possible to trim using all possible pin combinations and, in each case, the current gain of the transistor is systematically adjusted by the TECH-TRIM techniques. Similarly, it is possible to trim, for example, JFETs as shown in Table 26.

Experiments have also been conducted which demonstrate the utility of TECH-TRIM for adjusting important parameters of integrated circuits. Consider, for example, the typical operational amplifier sketched in Figure 31. An important specification for this circuit, and one that is easy to trim, is Vio. For the electrical configuration shown in Figure 31, it is convenient to trim between the collector and base on either transistor Q_1 or Q_2. Further note that such trimming can be done after the part is packaged by exercising the Vcc line and the appropriate input. Trimming Q_1, for instance, makes Vio less positive, or more negative. To this end, Table 27 summarizes each of the six possible results that can be achieved. It is recognized, of course, that trimming of Vio is normally done in order to decrease the magnitude of this parameter. Table 28 contains examples of trimming Vio into the tens of microvolts range and Table 29 shows how TECH-TRIM can achieve sub-microvolt offsets.

Similar capabilities exist for integrated circuits having different configurations. For example, many operational amplifiers with PNP inputs are easily trimmed using the Vee line and the corresponding input. For parts where the region to be trimmed is buried internal to the chip, access can be gained by adding auxiliary trimming pads or by using current steering diodes and related techniques.[47]

In addition to providing the capability to adjust devices and circuits, it is also imperative that the trim technology results in reliable and stable product. One way of assessing the reliability of a process is to examine its effect on the low frequency noise characteristics of a device. An increase in low

Sample No.	Pre-Trim Beta	Post-Trim Beta	Remarks
1	200	134	E-B Trim
2	166	150	C-E Trim
3	240	200	E-C Trim
4	200	160	C-B Trim

Table 25. An Illustration Of Several Ways To Trim A Bipolar Transistor.

No.	Pre-Trim I_{DSS}	Post-Trim I_{DSS}	Pre-Trim G_M	Post-Trim G_M	Remarks
1	4.13 mA	4.50 mA	3.90 mS	3.75 mS	D-S Trim
2	1.33 mA	1.45 mA	2.50 mS	2.25 mS	S-D Trim
3	1.50 mA	1.52 mA	2.50 mS	2.45 mS	G-D Trim

Table 26. An Illustration Of Several Ways To Trim A JFET.

Sample No.	Pre-Trim V_{io}	Post-Trim V_{io}	What Was Demostrated
1	+6.7 mV	+17.9 mV	Trimmed positive value to a larger positive value
2	+12.8 mV	+750 μV	Trimmed positive value to a smaller positive value
3	+2.5 mV	-860 μV	Trimmed positive value through zero to a negative value
4	-1.9 mV	-6.1 mV	Trimmed negative value to a larger negative value
5	-1.3 mV	-50 μV	Trimmed negative value to a smaller negative value
6	-7.7 mV	+320 μV	Trimmed negative value through zero to a positive value

Table 27. A Demonstration Of Each Of The Six Possible Cases Resulting From Trimming The Input Offset Voltage Of An Operational Amplifier.

Sample No.	Pre-Trim V_{io}	Post-Trim V_{io}
1	+0.26 mV	-30 μV
2	-1.30 mV	-50 μV
3	+1.82 mV	-70 μV

Table 28. Trimming Of V_{io} Into The Tens Of Microvolts Range.

Sample No.	Pre-Trim V_{io}	Post-Trim V_{io}
1	+1.8 mV	-0.8 μV
2	-0.8 mV	-0.7 μV

Table 29. Trimming Of V_{io} Into The Sub-Microvolt Range.

frequency noise is, frequently, an early warning indicator that the long term reliability of the part has been comprised.

The impact of TECH-TRIM on the low frequency noise of an operational amplifier has been assessed using the circuit presented in Figure 33. The series-coupling capacitor, C, prevents dc bias from getting into the instrumentation, and should be large enough to pass noise components having a frequency of a few hertz. Table 30 compares the RMS noise output of a number of operational amplifiers before and after trimming. Notice that trimming does not have a detrimental effect on the noise performance. Also, note on unit 2 a substantial and erratic noise component before trimming. This is, probably, a consequence of a chip manufacturing flaw such as oxide in a contact opening or a marginal wire bond. Interestingly, trimming unit 2 repairs this manufacturing flaw, in addition to tweaking the Vio of the amplifier.

Another way of evaluating the noise performance is with a low frequency spectrum analyzer. The results of such a test are summarized in Table 31 and, again, show that TECH-TRIM has no undesired effect on the noise characteristics of the part.

An independent evaluation of the stability characteristics of parts which have been trimmed is presented in Table 32. In these experiments, a Vio-trimmed operational amplifier is exercised under normal bias at room temperature and Vio is measured at frequent intervals. It is apparent that the Vio changes somewhat immediately after the packaged part is inserted into the test jig. This is presumed to occur while the device is mechanically relaxing and thermally equilibrating and does not represent a fundamental limitation of TECH-TRIM. Such a supposition is supported by the data points at 45 hours which, apparently, show a fixture-chip transient immediately after re-insertion. In any event, it is observed that the offset voltage has no tendency to return to its pre-trim value during the 168 hour life test.

Finally, Table 33 summarizes the results of an accelerated shelf life test conducted on both trimmed and untrimmed amplifiers. Assuming an Arrhenius dependence with an activation energy of 1 eV, the conditions of this test are equivalent to 214 years at room

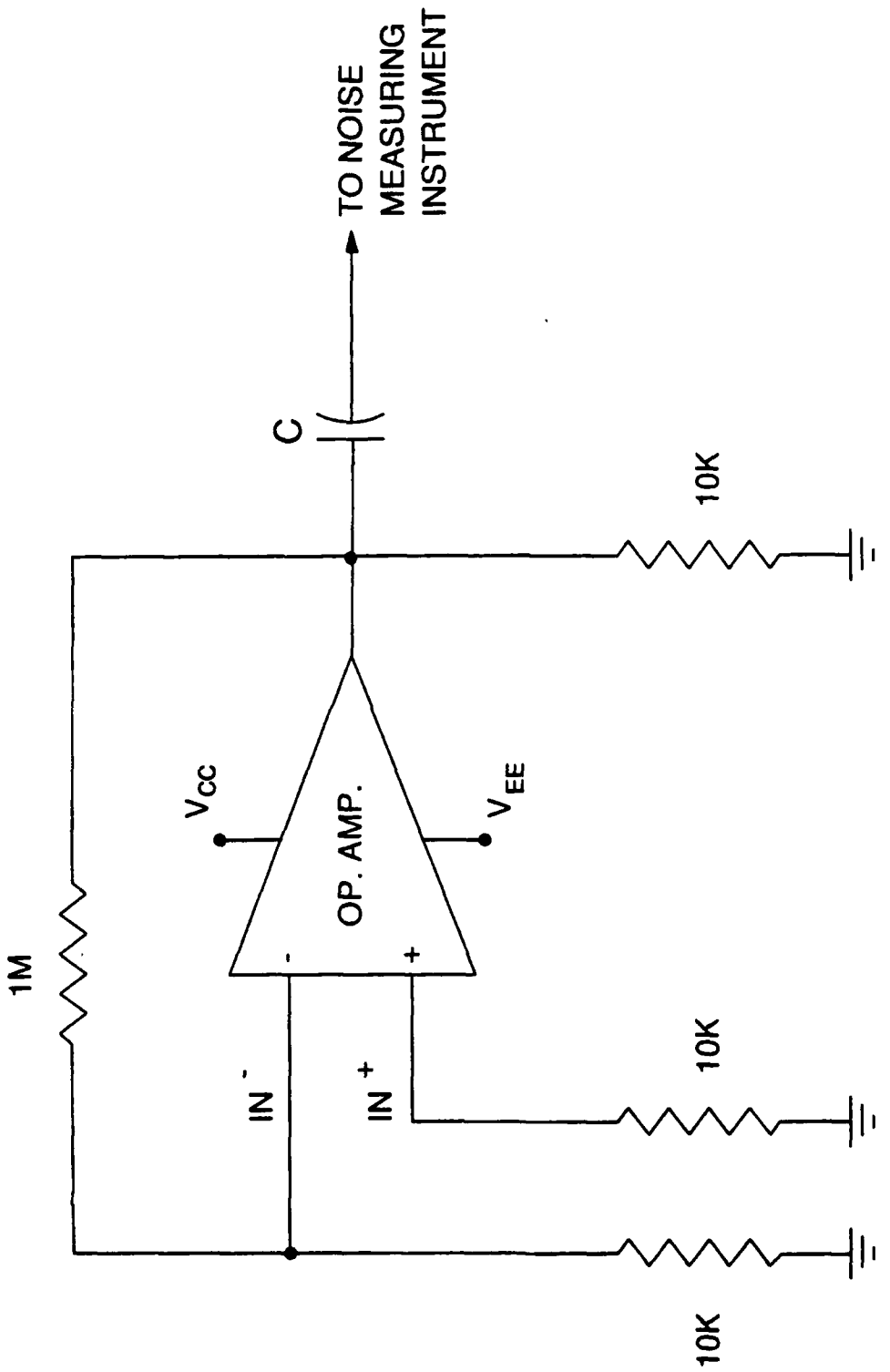

Figure 33. An Example Of A Noise Measuring Circuit.

Unit	RMS Output Before Trim	RMS Output After Trim
1	0.48 mV	0.46 mV
2	~ 5 mV (jumpy)	0.45 mV
3	0.62 mV	0.66 mV
4	0.47 mV	0.47 mV
5	0.46 mV	0.46 mV

Table 30. Noise Performance Of Operational Amplifiers As Measured With An HP 3400A RMS Voltmeter.

Frequency		Noise Magnitude Before Trim	Noise Magnitude After Trim
10.75	Hz	-73 dB	-73 dB
100	kHz	-93 dB	-93 dB

Table 31. Noise Performance Of An Operational Amplifier As Measured With An HP 3561A Dynamic Signal Analyzer.

Elapsed Time	Event	Measured V_{io}
-10 seconds	Inserted virgin device into test socket	+1.53 mV
0 seconds	Trimmed circuit	---
10 seconds	Inserted trimmed device into test socket	+0.73 mV
30 seconds		+0.70 mV
0.5 hours		+0.70 mV
21 hours		+0.70 mV
45 hours		+0.71 mV
45 hours, 10 seconds	Removed device and re-inserted	+0.74 mV
45 hours, 25 seconds		+0.71 mV
117 hours		+0.71 mV
141 hours		+0.71 mV
168 hours	Test terminated	+0.71 mV

Table 32. Results Of A 168 Hour Life Test On A Trimmed Operational Amplifier.

Sample No.	Trimmed?	Initial V_{io}	Final V_{io}
1	No	-0.05 mV	-0.06 mV
2	No	+1.67 mV	+1.70 mV
3	Yes	+0.88 mV	+0.89 mV
4	No	+1.37 mV	+1.39 mV
5	Yes	-3.09 mV	-2.77 mV
6	Yes	+0.46 mV	+0.46 mV
7	Yes	+0.02 mV	+0.02 mV
8	No	+2.96 mV	+2.95 mV
9	Yes	+0.76 mV	+0.76 mV
10	No	+3.62 mV	+3.64 mV
11	Yes	-3.23 mV	-3.18 mV
12	No	+0.09 mV	+0.07 mV

Table 33. Results Of A 24 Hour Accelerated Shelf Life Test At 150°C. (Assuming An Arrhenius Relationship With An Activation Energy Of 1 eV, This Is Equivalent To 214 Years At 27°C).

temperature. Note, by comparison of the trimmed and untrimmed components, that trimming does not aggravate the drift in the measured parameter.

4.5.5 Implications of the TECH-TRIM Technology

It is apparent that TECH-TRIM enjoys features that make it immediately applicable to a host of important integrated circuit problems. A synopsis of selected characteristics and implications of TECH-TRIM is presented in Tables 34-38.

4.5.6 Computer Control of the TECH-TRIM Process

The three generic routines detailed in Figures 34-36 illustrate trimming of a sample parameter and capture the essence of how to program a computer-driven tester to perform TECH-TRIM. The nomenclature employed in these example programs is defined in Table 39.

Can employ equipment already available on the production floor

Permits a continuous range of trimming

Requires little or no increase in die size over a similar, untrimmed chip

Trimming area overhead is independent of the trim precision desired

Provides capability to trim out assembly shift on packaged parts

Table 34. Selected Implications Of TECH-TRIM For Manufacturing.

Can use less skilled production operators in the probing and test areas

Can control inventory by trimming only to the specifications required by the warehouse

Can do real time inventory control by tying field offices directly into the probe and test areas

Can source several products from the same set of masks

Table 35. Selected Implications Of TECH-TRIM For Production Control.

Can dynamically skew the yield distribution to trade-off selling price and market share

Can combat price-fixing at no incremental cost to the factory

Can run precision products on less expensive wafer flows

Table 36. Selected Implications Of TECH-TRIM For Finance.

Can dynamically adjust value added to the product at no incremental cost to the factory

Can issue data sheets with guaranteed values, rather than typical values

Can disguise the method of making performance improvements from the competition

Table 37. Selected Implications Of TECH-TRIM For Strategic Marketing.

Can successfully employ less accurate computer-aided design models at the design stage

Can easily customize parts sourced from the same mask set

Can tweak, for example, the on-board clock on digital circuits

Can enhance the bit resolution of data conversion products

Can improve the matching of small, fast devices

Can include on-board circuitry which allows the chip to tweak itself

Can afford a customer the possibility of field adjustment and repair

ıble 38. Selected Implications Of TECH-TRIM For Product Definition.

```
Begin

   Setup (UUT, fixture, sensors, supplies);

   Pulse (trim_pin[n]); [send to component
                          needing to be trimmed]

End.
```

Figure 34. First Example Trim Program.

```
Begin

   Setup (UUT, fixture, sensors, supplies);

   N:=1

   Measure (trim_parameter[n]);

   While trim_parameter[n]>trim_spec[n] AND
                  N<Nmax DO

      Pulse (trim_pin[n]); [send to component
                                 needing to be trimmed]

      Measure (trim_parameter[n]);

      N:=N+1

   End;

End.
```

Figure 35. Second Example Trim Program.

```
Begin

    Setup (UUT, fixture, sensors, supplies);

    N:=1

    While trim_parameter[n]>trim_spec[n] AND
                    N<Nmax DO

        Pulse (trim_pin[n]); [send to component
                                needing to be trimmed]

        Measure (trim_parameter[n]);

        N:=N+1

    End;

End.
```

Figure 36. Third Example Trim Program.

ACRONYMS

UUT (unit under test)

VARIABLES

Trim_pin[n]	[points of electrical access to the device to be trimmed]
Trim_parameter[n]	[measured value of parameter(s) which may be adjusted by the trimming process]
Trim_spec[n]	[measured electrical specifications which may be achieved by the trimming process]
Nmax	[maximum allowed number of attempts to trim to a particular specification]

PROCEDURES

Setup (UUT, fixture, sensors, supplies)	[makes connections to, and provides the electrical stimulus for the UUT and, in addition, measures all of the necessary parameters]
Pulse (trim_pin)	[generates and directs an appropriate electrical trimming pulse(s) to the specified trim pin(s)]
Measure (trim_parameter)	[measures any desired electrical parameter(s) of the UUT]

Table 39. Definition Of Terms Used In Figures 34-36.

5.0 SOME WAYS TO OBTAIN IMPROVED TRACKING OF MODULES WITHIN THE ARRAY

The performance of a radar transmit/receive module is a function of the module's physical position in the array and of the instantaneous gain and phase setup of the surrounding modules. In addition, array temperature gradients and vehicle flexure will perturb the accuracy of selected modules. Consequently, modules that have been identically manufactured will not necessarily perform identically when they are assembled into an active, phased array.

Certainly, providing improved means for the modules to adapt to their array environment is of interest. Some of the possible techniques involve open-loop correction schemes while more complicated perturbations necessitate the use of closed-loop, negative feedback methods.

5.1 Open-Loop Module Control

Many of the open-loop module control technologies being employed on contemporary arrays are, essentially, a way of calibrating the respective modules in the system. Sometimes this calibration involves two, separate steps. The first is to exercise an individual module on the bench and, thus, identify whatever calibration is required to make all such modules identical. Subsequently, these modules are assembled into an array and the entire array is calibrated. The array can be calibrated for variations in a number of environmental factors and a few of these factors are identified in Table 40. The array calibration can, obviously, be based upon either far-field or near-field measurements. Regardless of the details, the calibration measurements are used to calculate a matrix of correction coefficients for each module in the array. These coefficients may be conveniently stored in read-only memory (ROM) chips co-located on the array platform itself.

A major advantage of open-loop module control is its simplicity.[3] Furthermore, research has demonstrated that the

Temperature

Frequency

Gain

Phase

Physical Location

Table 40. Some Sources Of Module Variations For Which Calibration Coefficients Have Been Provided.

open-loop approach can achieve reasonable performance for certain types of calibration. Figure 37, for example, illustrates a significant improvement in gain error as a consequence of providing open-loop temperature compensation for an individual module.[3] Similar approaches using both temperature and power calibration have resulted in individual modules enjoying ± 0.5 degrees in phase tracking and ± 0.08 decibels of gain error.

Another open-loop method of improving the performance of a radar array involves the use of logarithmic amplifiers.[48] Such an amplifier generates an output voltage that is proportional to the logarithm of the input voltage. An illustration of how this function might be implemented in hardware is shown in Figure 38. In this configuration, identical gain stages are cascaded and detectors are located at the indicated nodes. Consequently, a logarithmic response results if each stage amplifier features a threshold below which the gain is a fixed value and above which the incremental gain is one. Clearly, such a logarithmic amplifier translates a wide input range into a much narrower range by capitalizing on the logarithmic transfer function. Thus, the technique yields a large dynamic range system without suffering the delay which would be incurred with a closed-loop, automatic gain control (AGC) circuit. Ultimately, of course, the dynamic range is limited by saturation on one side and noise on the other.

It is apparent that open-loop techniques can improve the performance of phased array radars. Unfortunately, open-loop technologies provide no feedback of pseudo-random fluctuations in the array environment. Consequently, they cannot address beam-forming problems caused by, for example, flexure of the array support vehicle.

5.2 Closed-Loop Module Control

Closed-loop control requires the use of a feedback path as illustrated in Figure 39. The general idea is to sample some parameter of the output and use an appropriate component of this signal to influence the overall response of the loop. Often this

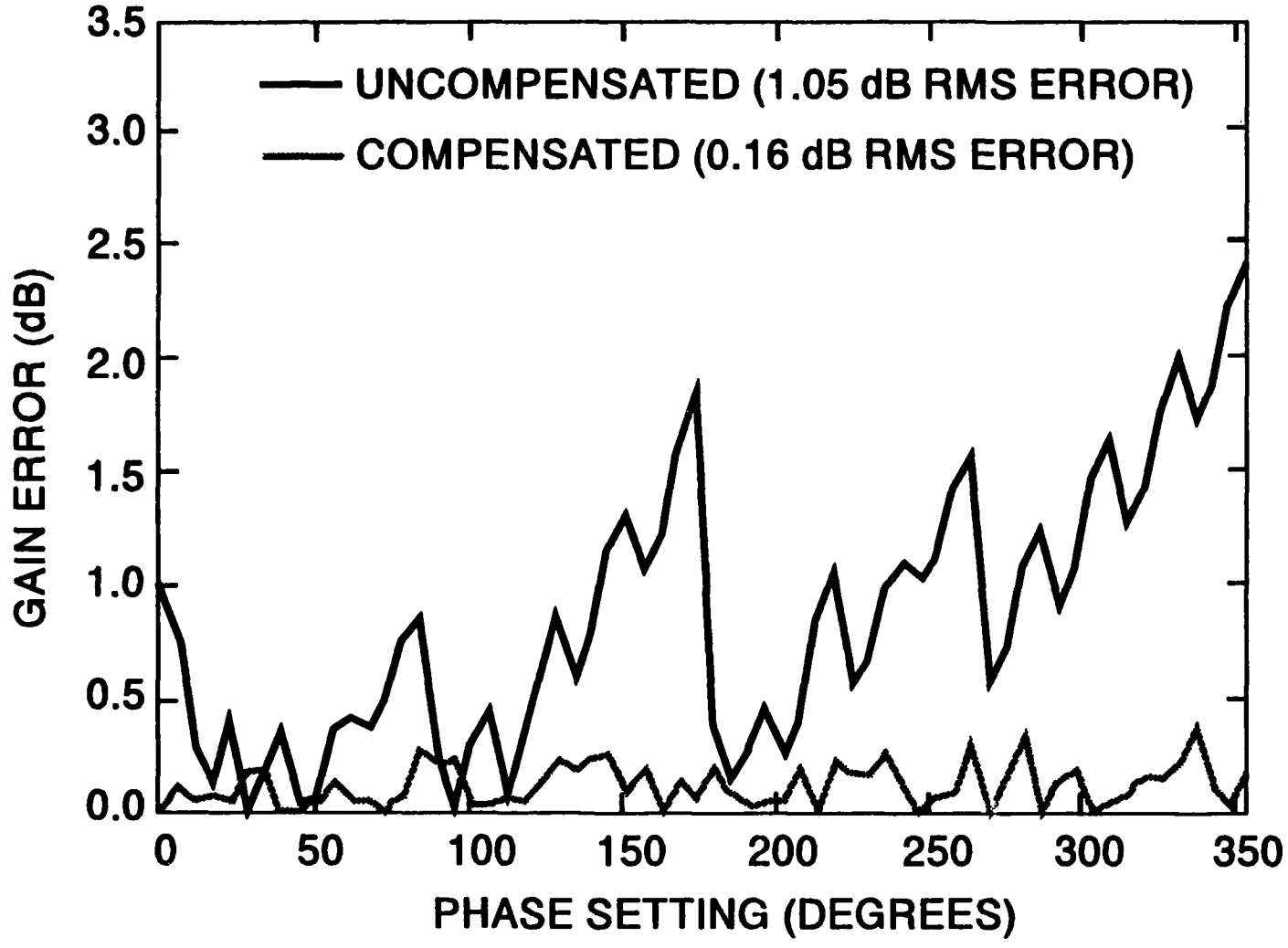

Figure 37. Gain Error Versus Phase Setting Of An Individual T/R Module Featuring Open-Loop Temperature Compensation At 27° C. (After Chilton, Reference 3).

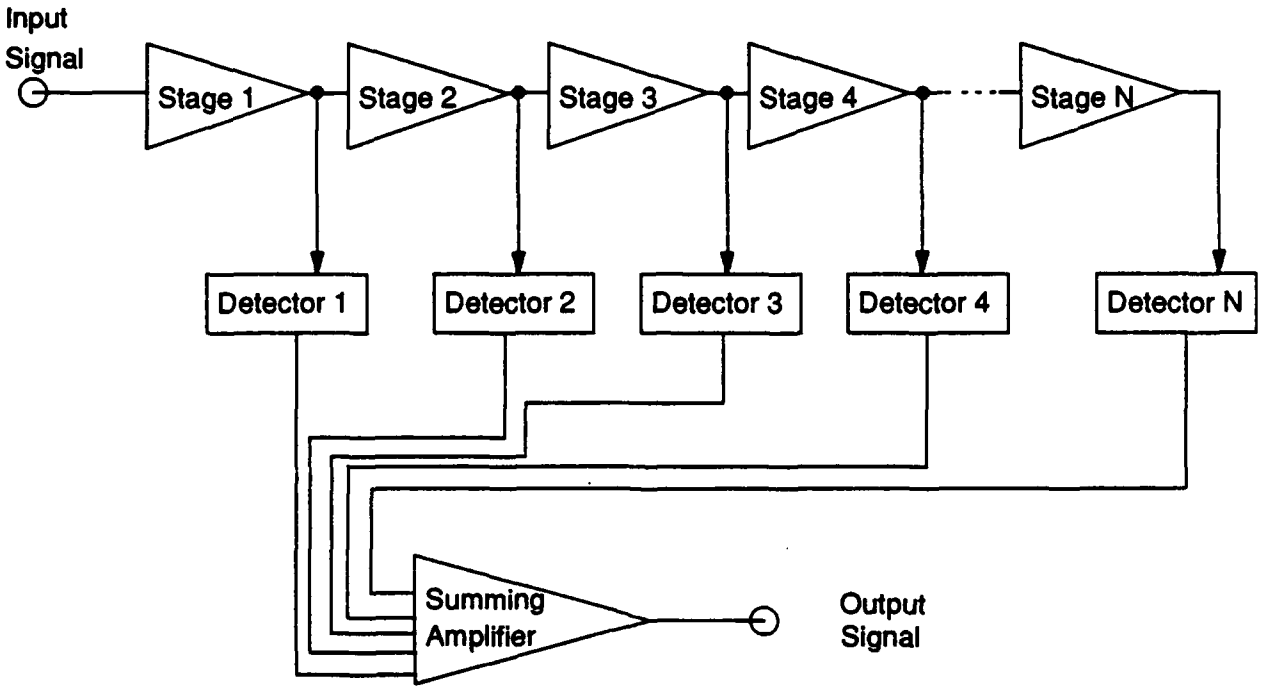

Figure 38. Schematic Illustration Of The Basic Principles Of Logarithmic Amplification.

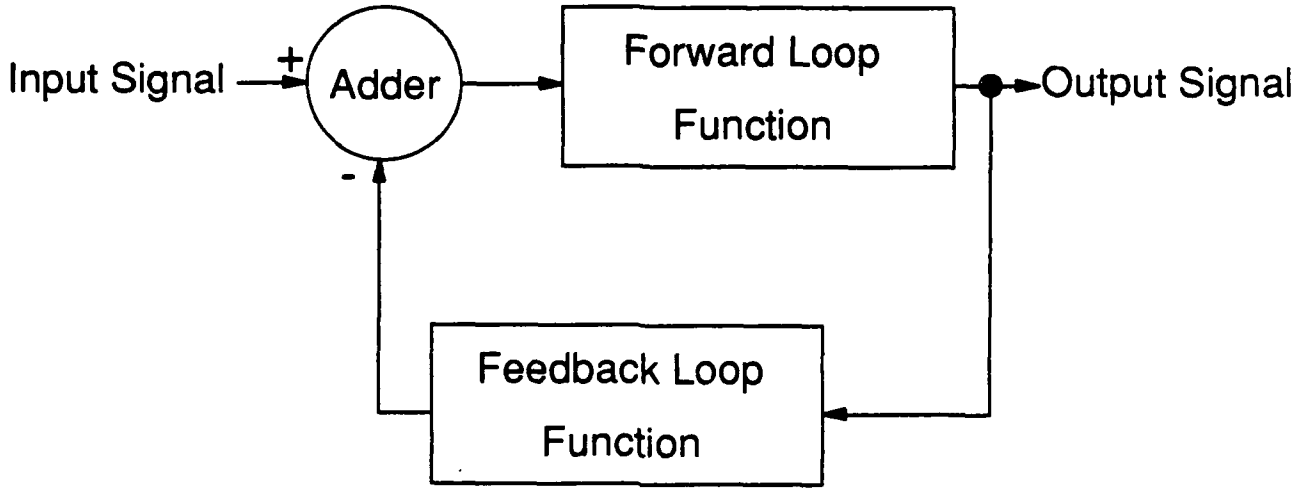

Figure 39. Schematic Representation Of A Negative Feedback Control System.

control signal is subtracted from the input stimulus giving rise to the term "negative feedback."

For phased array radars, there are two feedback loops of practical interest and these are summarized in Table 41. In one case, some output of a module is locally sampled and this information is, then, used to control that module. Alternatively, the performance of the array itself can be sampled and converted to a form appropriate for the control of the appropriate modules.

An example of using module output to control module performance is the automatic gain control loop illustrated in Figure 40. This hardware is pertinent to receiver systems and might be employed while a T/R module is in the receive mode. In this AGC circuit, the output signal is adjusted in amplitude by a pair of cascaded amplifiers, one of which has variable gain. A portion of that same output signal is sampled, filtered to remove amplitude modulation effects and injected into a difference amplifier. This difference amplifier compares the resulting amplitude to a preset reference level and derives a control signal which is, then, employed to adjust the gain of the indicated amplifier stage.

Similar feedback circuits can be used to control the frequency response, decrease distortion, improve linearity and increase the dynamic range of receivers. Recall, for instance, the value of providing the capability to tweak high frequency integrated circuits after they have been fabricated as discussed in Section 4.5. This tweaking, or trimming, is seen to cause permanent changes to the response of the constituent circuit. For example, perusal of Figure 27 confirms that a permanent adjustment of the quiescent point of an amplifier can alter the scattering parameters of the requisite transistors and, thus, improve the overall response of the system itself. An interesting variation on this theme might be to provide the means to do such quiescent point tweaks adaptively on a continuous, real time basis. In this case, dedicated circuitry can be included to monitor the system performance and make the appropriate bias adjustments via a feedback loop as shown in Figure 41. Knowledge of the correct

Feed Back Module Data Into The Module

Feed Back Array Data Into The Module

Table 41. Two Feedback Loops Appropriate For Closed-Loop Module Control.

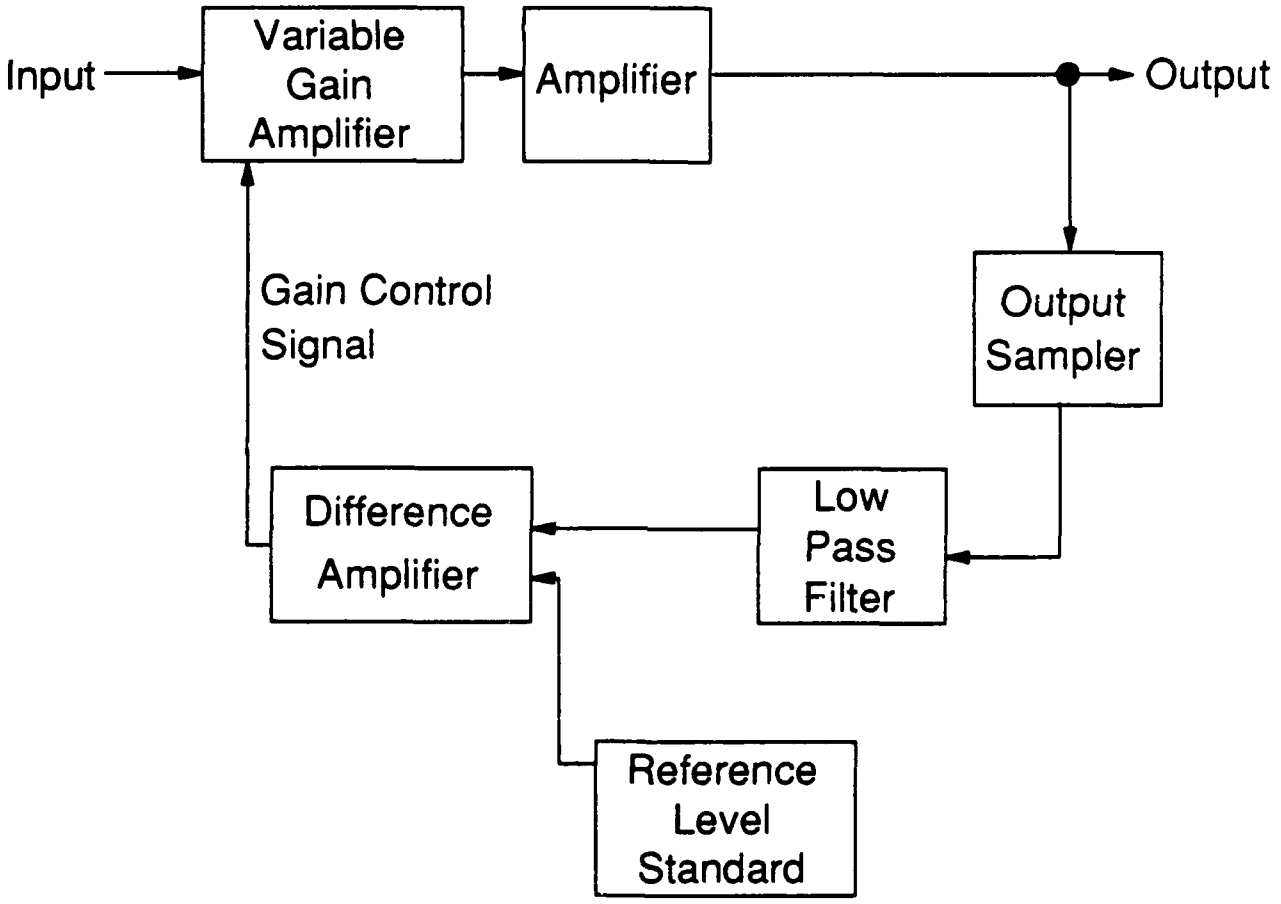

Figure 40. An Automatic Gain Control Loop For A Receiver.

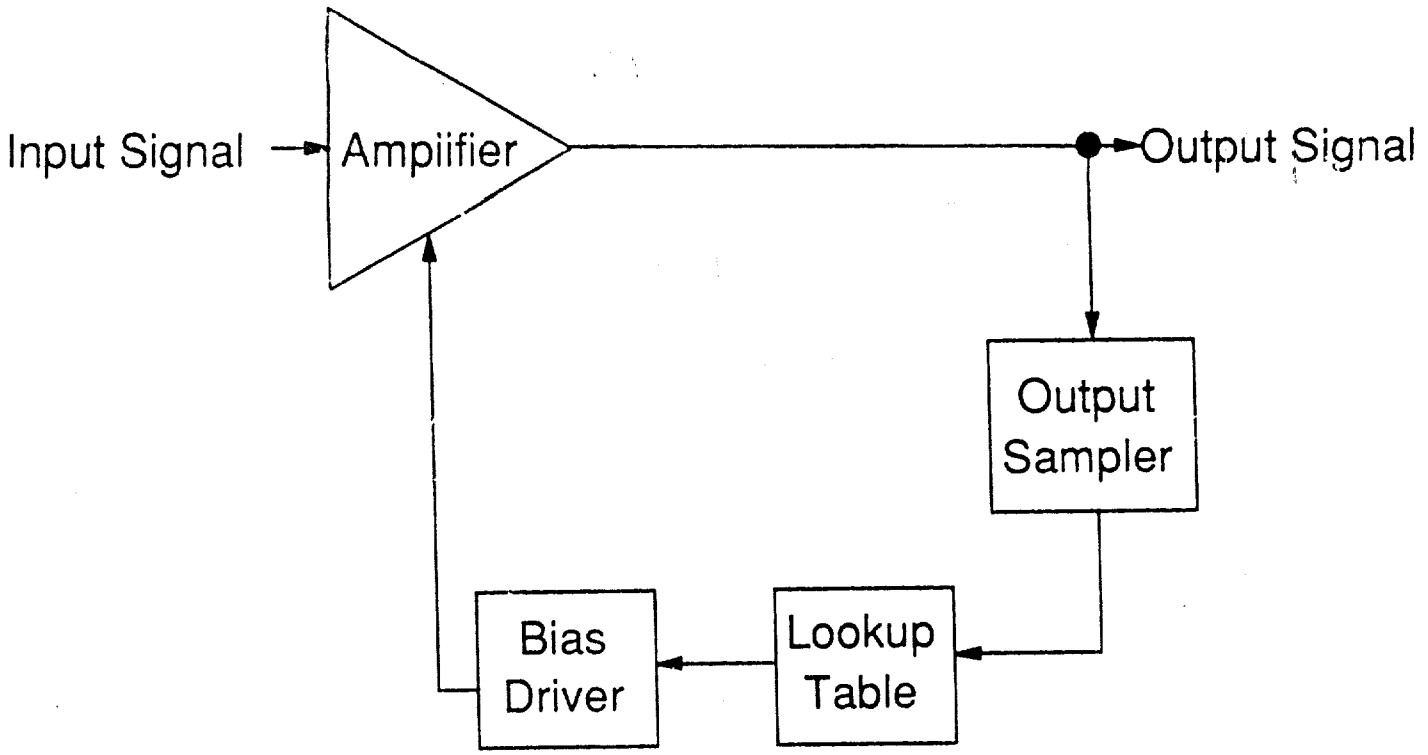

Figure 41. A Circuit For Adjusting The Performance Of An Amplifier By Adaptively Controlling Its Bias Point.

adjustment for various circuit maladies can be accrued via design simulations or early production testing. In either event, the appropriate coefficients can be stored in an on-board lookup table for easy access in the field.

An integrated system with such capability can dynamically reconfigure itself in an optimum way. Consider, for example, the front end of a receiving system. If no signals are present, the circuit can adjust itself for maximum sensitivity. If in-band, large signals are present, the amplifier can be reconfigured for increased dynamic range.

The closed-loop methodology can, presumably, be extended to control the entire radar array. One possible way of doing this might involve locating field-sampling probes in the near-field pattern of the antenna as shown schematically in Figure 42. The information obtained by these probes could, then, be processed, analyzed and used to adjust the belligerent modules contributing to a sub-optimum array pattern.

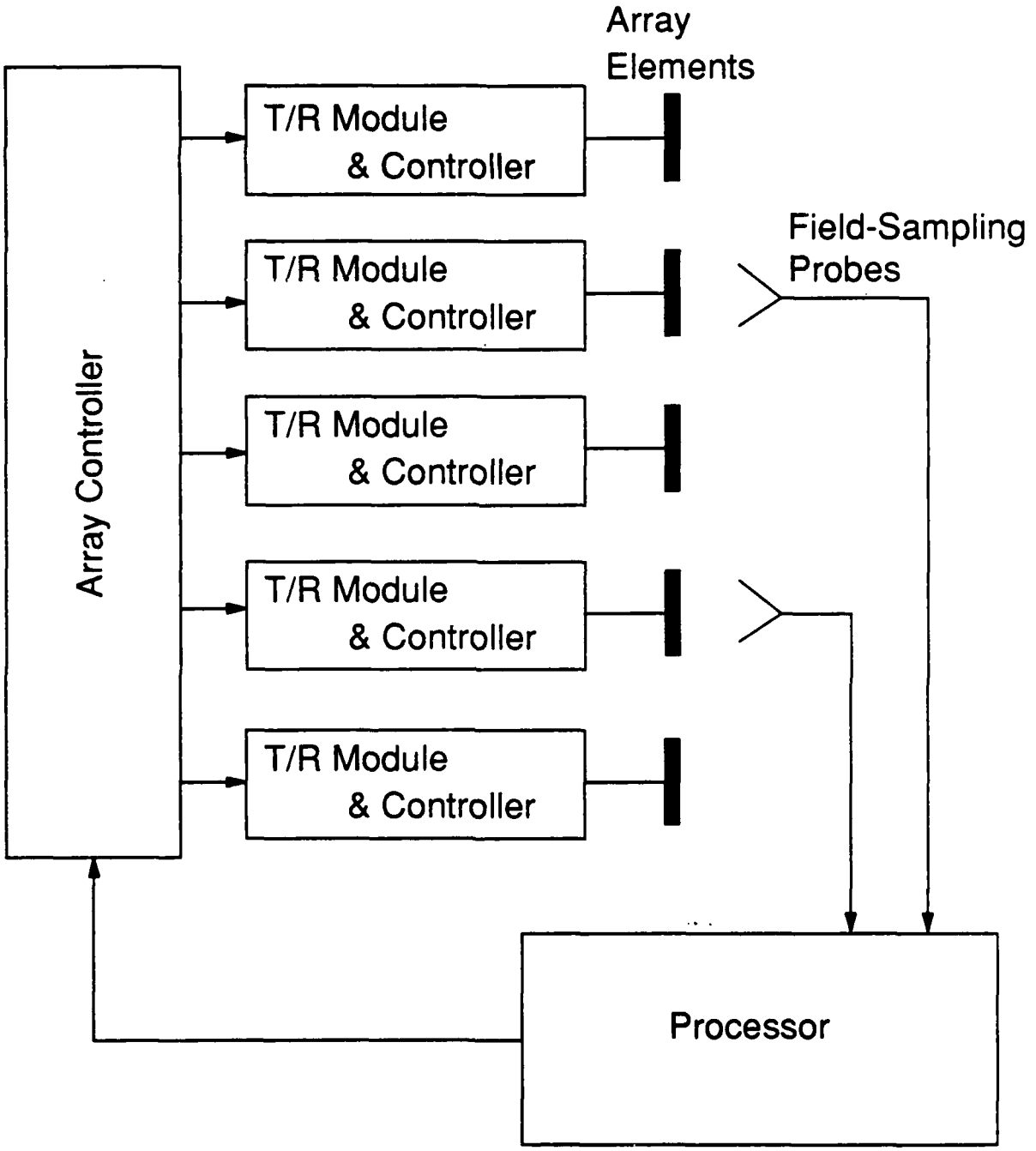

Figure 42. Schematic Representation Of A Closed-Loop Array Control System.

6.0 AN INVESTMENT STRATEGY FOR UHF

6.1 Introduction and Requirements

This report has summarized some of the items currently limiting the performance of UHF transmit/receive radar modules. The missions envisioned by the Air Force require that the corresponding phased arrays feature low sidelobes and a high gain coefficient per unit of aperture. Consequently, very accurate control of the relative gains and phases of the radiating elements is required. Moreover, this gain and phase stability must be maintained over the ensemble of steering angles and observation frequencies. In addition to the rigorous amplitude and phase requirements, it is desired that the constituent receiver path enjoy an improved dynamic range.

Clearly, addressing these, and similar, performance improvement specifications involves a two-pronged approach as outlined in Table 42. Sections 6.2 and 6.3 suggest methods for obtaining more nearly identical modules. Section 6.4 compliments these ideas by recommending some ways to improve the ability of these modules to adapt to the dynamics of the array environment. Taken together, these sections constitute a technological investment strategy for UHF.

6.2 Module Componentry Investment Strategy

Georgia Tech believes that considerable effort should be devoted to the improvement of the components used to populate transmit/receive modules. Some of the areas where research may prove particularly fruitful are identified below.

- Employ silicon rather than gallium arsenide at UHF whenever possible. Capitalize on the greater yield, maturity and crystal quality of silicon.

- Use available transistors well below their maximum, specified frequency. Trade off this excess bandwidth for improved noise, gain, linearity, reliability and yield.

Make More Nearly Identical Modules

Provide Better Means For The Modules To Adapt To The Array Environment

Table 42. Two General Ways To Improve The Performance Of Phased Array Radars.

- Consider the employment of balanced circuitry internal to the system. Develop both unbalanced-to-balanced and balanced-to-unbalanced converters to support this system architecture.

- Eliminate the requirement to match every node to 50 ohms. Use impedances ranging from several ohms to several thousand ohms if convenient and practical.

- Develop push-pull amplifiers using MOS driver transistors. The MOSFET is a square-law device and, thus, properly matched devices running in this configuration will have no harmonic distortion.

- Develop improved power transistors and, also, better methods for power combining these transistors. Consider vertical, power devices including MOSFETs, SITs and SSTs. Although bipolar devices currently have the edge over MOS at UHF, this may not be so in the future. In either event, MOSFETs are easier to power combine.

- Employ low noise, high power transistors in the front end of receivers in an attempt to increase dynamic range.

- Track the progress of vacuum microelectronics and examine, in particular, the dynamic range, speed and integrability of the corresponding devices. At present, Henry F. Gray at NRL is a good resource on this technology.

- Optimize the level of integration of the components in the modules. For all but the highest power applications, the optimal level of integration is probably higher than that seen at the present time.

- Refine the etch and refill technique in order to permit the integration of vertical, power transistors with auxiliary circuitry.

- Consider the use of DIMMIC, ISOSAT and MOSAIC process flows to fabricate UHF radar module components. These technologies promise improved performance and increased levels of integration for frequencies up through, and well beyond, UHF.

- Continue the development of active circulators and similar techniques for allowing the isolation function to be more easily integrated onto desirable substrates.

- Develop oscillators which resonate at higher fundamental frequencies in an attempt to reduce the aggregate noise of the frequency source function. Similarly, build oscillators which can be driven harder and, thus, would have an improved carrier-to-noise ratio. Consider cryogenic oscillators, $LiTaO_3$ oscillators and similar, advanced technologies.

- Incorporate logarithmic circuitry in the receiver path in order to improve the dynamic range of the system.

6.3 Module Manufacturing Investment Strategy

Several improvements in module manufacturing methodologies hold promise for easing the burden of T/R module production. A compilation of such possibilities is enumerated below.

- Standardize a few wafer manufacturing processes and, then, design module hardware to yield well on these flows. Remember that "no product is worth its own process."

- Permit manufacturers to get further down the learning curve by increasing the volume on important products. Capitalize on standard manufacturing processes. Consider qualifying

commercial-grade and industrial-grade chips for military deployments.

- o Develop and utilize techniques for post-fabrication trimming of UHF devices and circuits. Investigate laser trimming, fuse blowing and electrical alteration technologies. Design-in the capability to trim the circuitry of interest and automate the requisite trimming algorithms, tests and hardware.

- o Develop a domestic source of low cost, high frequency packages to reduce the dependence on a Japanese supplier. In addition, investigate ways to assemble modules from bare, or package-less, components.

6.4 Module Control Investment Strategy

One aspect of module control involves the intentional placement of the array in a more favorable environment. Several ways of doing this are summarized below.

- o Pursue methods for reducing the mechanical flexure in the array support hardware. Similarly, develop techniques for isolating the array from vehicular vibrations.

- o Locate the array away from highly reflective surfaces on the support vehicle. Consider the use of a stealth platform for the array.

- o Increase the number of modules in the phased array. Previous research has suggested that performance tends to improve as approximately the square root of the number of modules in the array.

- o Provide improved means of regulating the supply voltages powering the array electronics. It has been shown that

power supply fluctuations can modulate the output of the radar transmitter.

- Continue to encourage the incorporation of open-loop correction methods.

- Re-visit closed-loop module control in an attempt to achieve the ultimate in array performance. Consider the use of adaptive, bias point tweaks to trade off the sensitivity and dynamic range of receiver systems. Similarly, investigate the use of switched emitter resistors or series limiters to adjust the output power of the transmitter function.

- Work on higher frequency operational amplifiers, processors, and similar control components to speed up the feedback control systems. Strive to achieve the required adjustments in only a few percent of the allotted dwell time.

- Investigate methods to do real time measurements and analysis of both array pattern and vehicular deflection. Consider the use of near-field probes and laser sensors, respectively. Optimize the resulting probe position and protocol.

- Acknowledge that future systems are likely to make more extensive use of digital techniques. Consequently, develop higher resolution and higher speed analog-to-digital and digital-to-analog converters. Increasing the number of bits translates to improved dynamic range while an escalation of the conversion frequency enhances the achievable range resolution.

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